

# High-Performance dsPIC33A Core with Floating-Point Unit, High-Speed ADCs and High-Speed PWM

## dsPIC33AK128MC106 Family



## Operating Conditions

- 3.0V to 3.6V: -40°C to +125°C, DC to 200 MHz

## High-Performance DSP/RISC CPU

- 32-bit Comprehensive Instruction Set for Optimized Speed and Program Code Size:
  - 16-bit dsPIC33 core compatible
  - Non-paged linear Data/Flash 24-bit addressing space
  - 16-bit/32-bit instructions for optimized code size and performance
- 32-Bit Wide Data Paths
- Single and Double Precision Floating-Point Unit (FPU) Coprocessor
- 2-Kbyte Instruction Cache
- 16-Bit/32-Bit Working Registers
- Dual 72-Bit Accumulators Supporting Fixed-Point DSP Operations
- Eight Level Deep Working Register Sets
- Eight Level Deep Accumulator Register Sets
- Eight Level Deep Floating-Point Register Sets

## Controller Features

- High-Current Sink/Source Capable I/Os
- Programmable Weak Pull-Up and Pull-Down Resistors
- Programmable Open-Drain Outputs
- Edge or Level Change Notification Interrupt on I/O pins
- Peripheral Pin Select (PPS) Remappable Pins to Reduce Board Layout Complexity
- Multiple Interrupt Vectors with Individual Programmable Priority
- Five External Interrupt Pins
- Selectable Oscillator Options Including:
  - 8 MHz, 1% at 0°C-85°C Internal Fast RC (FRC) oscillator
  - 8 MHz, 2% Internal Backup Fast RC (BFRC) oscillator with 32 kHz divided output
  - High-speed crystal resonator oscillator or external clock
- Two 1.6 GHz PLLs for Peripherals which can be clocked from the FRC or a Crystal Oscillator
- Reference Clock Output (REFO)
- Low-Power Modes (Sleep and Idle)
- Power-On Reset and Brown-Out Reset

## High-Speed PWM

- Four PWM Generators (Four Pairs with Eight Outputs)
- Up to 2.5 nS PWM Resolution
- Dead Time for Rising and Falling Edges
- Dead-Time Compensation Supports Lower Speed Operation
- Clock Chopping for High-Frequency Operation
- PWM Support for:
  - BLDC, PMSM, ACIM, SRM and stepper motors
- Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

## Two High-Speed Analog-to-Digital Converters

- 12-bit Resolution
- Up to 40 Msps Conversion Rate
- Up to 22 Analog Input Pins
- 20 Settings Channels. Each Channel:
  - Supports discrete configuration
  - Can be assigned to any analog input (I/O pin or internal signal)
  - Can be set to a different sampling time
  - Can be configured as single-ended or differential
  - Conversion result can be formatted as unsigned or signed
  - Conversion result can be left-aligned (fraction format)
  - Has a separate 32-bit conversion result register
- Supports Four Sampling Modes:
  - Oversampling of multiple samples
  - Integration of multiple samples
  - Window (multiple samples accumulated when the gate signal is active)
  - Single conversion
  - All channels have a digital comparator to detect when the conversion result is less than, greater than, in bounds or out of bounds for the configurable thresholds.
  - Three channels support second result accumulator to implement second order filters.
- Band Gap Reference and Temperature Sensor Diode Inputs

## Peripheral Features

- 3 Four-Wire SPI Modules (up to 40 Mbps):
  - 16-byte FIFO
  - Variable data width
  - I<sup>2</sup>S mode
- Two I<sup>2</sup>C Modules w/Address Masking and IPMI Support
- Three Protocol UARTs with 8-Character RX/TX FIFOs and Automated Handling Support for:

- LIN 2.2
- DMX
- Smart card (ISO 7816)
- IrDA<sup>®</sup>
- Two SENT Modules
- One Dedicated 32-Bit Timer/Counter
- Four Single Output Capture/Compare/PWM/Timer (SCCP) Modules:
  - Flexible configuration as PWM, input capture, output compare or timers
  - Two 16-bit timers or one 32-bit timer in each module
  - Single PWM output pin
- One Quadrature Encoder Interface (QEI):
  - Four inputs: Phase A, Phase B, Home and Index
- Four Configurable Logic Cells (CLC) with Internal Connections to Select Peripherals and PPS
- Serial Encoder Interface BiSS with up to Four Client Encoders Support
- Peripheral Trigger Generator (PTG):
  - Ten input trigger sources from other peripheral modules
  - Five output triggers to other peripheral modules
  - Four individual interrupt request signals
  - CPU independent state machine-based instruction sequencer

## Analog Features

- Three 5 nS Analog Comparators with 12-Bit PDM DACs:
  - Input multiplexing
  - Slope compensation
  - One DAC output buffer
- Three Rail-to-Rail 100 MHz Operational Amplifiers with:
  - 100 V/ $\mu$ S slew rate
  - 1 mV offset (typical)
- Four 10  $\mu$ A Constant Sources + Four Programmable Sources

## Safety Features

- Windowed Watchdog Timer (WDT)
- Deadman Timer (DMT)
- Four I/O Integrity Monitors (IOIM)
- Fail-Safe Clock Monitor (FSCM) with Automatic Switchover to Backup Clock Source with:
  - Programmable over-frequency/under-frequency thresholds
- Flash Error Correcting Code (ECC)
- RAM Error Correcting Code (ECC)
- RAM Memory Built-In Self-Test (MBIST)
- 32-Bit Cyclic Redundancy Check (CRC) Module
- Entire Flash OTP by ICSP<sup>™</sup> Write Inhibit

- Capless Internal Voltage Regulator
- Virtual PPS Pins for Redundancy and Monitoring
- Temperature Sensor Diode

## Security Module

- Secure Boot
- Secure Debug
- Immutable Root of Trust (IRT)
- Code Protect
- ICSP Program/Erase Disable (Entire Flash OTP by ICSP Write Inhibit)
- Firmware IP Protection
- Flash Write Protection

## Functional Safety

Functional Safety Readiness – ISO 26262/IEC 61508/IEC 60730

To learn about the Functional Safety Readiness of this device family and various Functional Safety standards an application can target using this device family, visit [www.microchip.com/dsPIC33-Functional-Safety](http://www.microchip.com/dsPIC33-Functional-Safety).

## Qualification

AEC-Q100 REV H:

- Grade 1: -40°C to +125°C
- Grade 0: -40°C to +150°C Planned

## Debug Features

- Three Programming and Debugging Interfaces:
  - Two-wire ICSP interface with non-intrusive access and real-time data exchange with application
- Five Complex and Five Simple Breakpoints
- IEEE Standard 1149.2 Compatible (JTAG) Boundary Scan

## dsPIC33AK128MC106 Product Family

The dsPIC33A family names, pin counts, memory sizes and peripheral availability of each device are listed in [Table 1](#), and their pinout diagrams are included as well.

**Table 1. dsPIC33AK128MC106 Family**

| Product           | Pins | Program Memory (Kbytes) | Data Memory (Kbytes) | General Purpose I/O/PPS | High-Resolution PWM (Generator Pairs) | Two 12-bit ADCs (External Analog Inputs) | Remappable Peripherals  |      |      |         |     |                      |      |     | Op Amplifiers | Comparators | 12-bit DACs | I <sup>2</sup> C | 32-bit CRC | DMA (Channels) | Packages  |
|-------------------|------|-------------------------|----------------------|-------------------------|---------------------------------------|------------------------------------------|-------------------------|------|------|---------|-----|----------------------|------|-----|---------------|-------------|-------------|------------------|------------|----------------|-----------|
|                   |      |                         |                      |                         |                                       |                                          | Dedicated 32-bit Timers | UART | BISS | SCCP(1) | CLC | SPI/I <sup>2</sup> S | SENT | QEI |               |             |             |                  |            |                |           |
| dsPIC33AK32MC102  | 28   | 32                      | 8                    | 19/19                   | 4*2                                   | 11                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 2             | 3           | 3           | 2                | 1          | 6              | SSOP/VQFN |
| dsPIC33AK32MC103  | 36   | 32                      | 8                    | 27/27                   | 4*2                                   | 15                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN      |
| dsPIC33AK32MC105  | 48   | 32                      | 8                    | 35/35                   | 4*2                                   | 18                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN/TQFP |
| dsPIC33AK32MC106  | 64   | 32                      | 8                    | 49/49                   | 4*2                                   | 22                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN/TQFP |
| dsPIC33AK64MC102  | 28   | 64                      | 16                   | 19/19                   | 4*2                                   | 11                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 2             | 3           | 3           | 2                | 1          | 6              | SSOP/VQFN |
| dsPIC33AK64MC103  | 36   | 64                      | 16                   | 27/27                   | 4*2                                   | 15                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN      |
| dsPIC33AK64MC105  | 48   | 64                      | 16                   | 35/35                   | 4*2                                   | 18                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN/TQFP |
| dsPIC33AK64MC106  | 64   | 64                      | 16                   | 49/49                   | 4*2                                   | 22                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN/TQFP |
| dsPIC33AK128MC102 | 28   | 128                     | 16                   | 19/19                   | 4*2                                   | 11                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 2             | 3           | 3           | 2                | 1          | 6              | SSOP/VQFN |
| dsPIC33AK128MC103 | 36   | 128                     | 16                   | 27/27                   | 4*2                                   | 15                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN      |
| dsPIC33AK128MC105 | 48   | 128                     | 16                   | 35/35                   | 4*2                                   | 18                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN/TQFP |
| dsPIC33AK128MC106 | 64   | 128                     | 16                   | 49/49                   | 4*2                                   | 22                                       | 1                       | 3    | 1    | 4       | 4   | 3                    | 2    | 1   | 3             | 3           | 3           | 2                | 1          | 6              | VQFN/TQFP |

**Note:**

- SCCP can be configured as a PWM with one output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

## Pin Diagrams

Figure 1. 28-Pin SSOP

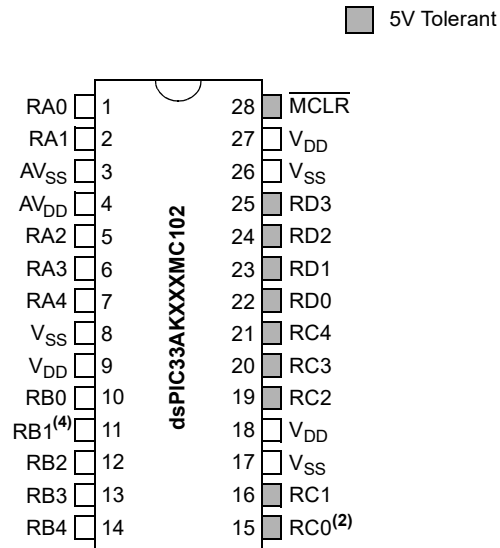


Table 2. 28-Pin SSOP Complete Pin Function Descriptions<sup>(1,3)</sup>

| Pin | Function                                                           | Pin | Function                                         |
|-----|--------------------------------------------------------------------|-----|--------------------------------------------------|
| 1   | PGD2/AD2AN6/CMP3C/ISRC2/IBIAS2/ <b>RP1</b> /SDA2/IOMF2/RA0         | 15  | OSCO/CLKO/ <b>RP33</b> /IOMF5/RC0 <sup>(2)</sup> |
| 2   | PGC2/DACOUT1/AD1AN7/AD2AN3/CMP1D/CMP2D/CMP3D/ <b>RP2</b> /SCL2/RA1 | 16  | OSCI/CLKI/ <b>RP34</b> /IOMF6/RC1                |
| 3   | AV <sub>SS</sub>                                                   | 17  | V <sub>SS</sub>                                  |
| 4   | AV <sub>DD</sub>                                                   | 18  | V <sub>DD</sub>                                  |
| 5   | OA1OUT/AD1AN0/CMP1A/ <b>RP3</b> /RA2                               | 19  | PGC3/ <b>RP35</b> /PWM4H/RC2                     |
| 6   | OA1IN-/AD1ANN1/AD2AN0/ <b>RP4</b> /RA3                             | 20  | PGD3/ <b>RP36</b> /PWM3H/IOMD0/RC3               |
| 7   | OA1IN+/AD1AN1/CMP1B/ <b>RP5</b> /RA4                               | 21  | <b>RP37</b> /PWM3L/IOMD1/RC4                     |
| 8   | V <sub>SS</sub>                                                    | 22  | <b>RP49</b> /PWM2H/IOMD2/RD0                     |
| 9   | V <sub>DD</sub>                                                    | 23  | TCK/ <b>RP50</b> /PWM2L/IOMD3/RD1                |
| 10  | OA2OUT/AD2AN1/CMP2A/ <b>RP17</b> /INT0/RB0                         | 24  | TDO/ <b>RP51</b> /PWM1H/IOMD4/RD2                |
| 11  | TMS/OA2IN-/AD1AN4/AD2ANN1/ <b>RP18</b> /RB1 <sup>(4)</sup>         | 25  | TDI/ <b>RP52</b> /PWM1L/IOMD5/RD3                |
| 12  | OA2IN+/AD2AN4/CMP2B/ <b>RP19</b> /RB2                              | 26  | V <sub>SS</sub>                                  |
| 13  | PGD1/AD1AN5/CMP1C/ISRC0/IBIAS0/ <b>RP20</b> /SDA1/RB3              | 27  | V <sub>DD</sub>                                  |
| 14  | PGC1/AN2AN5/CMP2C/ISRC1/IBIAS1/ <b>RP21</b> /SCL1/RB4              | 28  | MCLR                                             |

**Note:**

1. **RPn** represents remappable peripheral functions.
2. This pin has 8x drive strength.
3. Unless otherwise stated, pins are 4x drive strength. Refer to Electrical Specifications for current drive strength details.
4. A pull-up resistor is connected to this pin when device is erased (JTAG enabled) and during programming.

## Pin Diagrams

Figure 2. 28-Pin VQFN

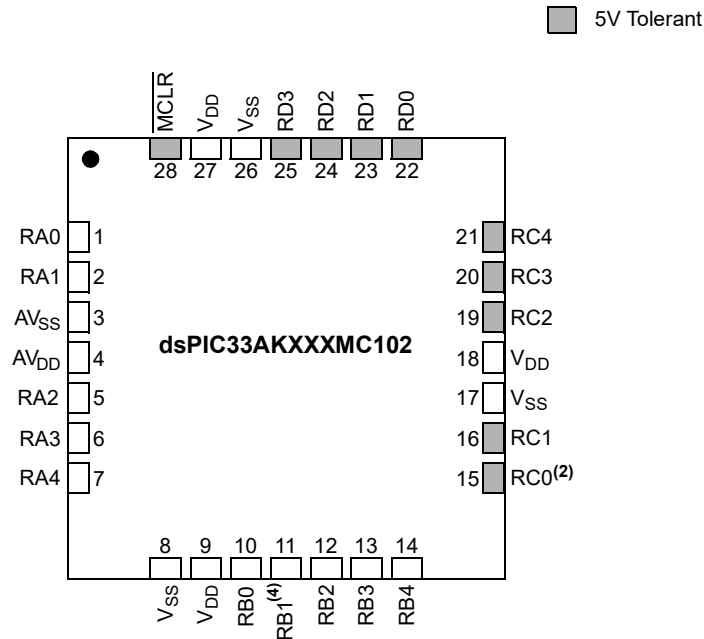


Table 3. 28-Pin VQFN Complete Pin Function Descriptions<sup>(1,3)</sup>

| Pin | Function                                                           | Pin | Function                                         |
|-----|--------------------------------------------------------------------|-----|--------------------------------------------------|
| 1   | PGD2/AD2AN6/CMP3C/ISRC2/IBIAS2/ <b>RP1</b> /SDA2/IOMF2/RA0         | 15  | OSCO/CLKO/ <b>RP33</b> /IOMF5/RC0 <sup>(2)</sup> |
| 2   | PGC2/DACOUT1/AD1AN7/AD2AN3/CMP1D/CMP2D/CMP3D/ <b>RP2</b> /SCL2/RA1 | 16  | OSCI/CLKI/ <b>RP34</b> /IOMF6/RC1                |
| 3   | AV <sub>SS</sub>                                                   | 17  | V <sub>SS</sub>                                  |
| 4   | AV <sub>DD</sub>                                                   | 18  | V <sub>DD</sub>                                  |
| 5   | OA1OUT/AD1AN0/CMP1A/ <b>RP3</b> /RA2                               | 19  | PGC3/ <b>RP35</b> /PWM4H/RC2                     |
| 6   | OA1IN-/AD1ANN1/AD2AN0/ <b>RP4</b> /RA3                             | 20  | PGD3/ <b>RP36</b> /PWM3H/IOMD0/RC3               |
| 7   | OA1IN+/AD1AN1/CMP1B/ <b>RP5</b> /RA4                               | 21  | <b>RP37</b> /PWM3L/IOMD1/RC4                     |
| 8   | V <sub>SS</sub>                                                    | 22  | <b>RP49</b> /PWM2H/IOMD2/RD0                     |
| 9   | V <sub>DD</sub>                                                    | 23  | TCK/ <b>RP50</b> /PWM2L/IOMD3/RD1                |
| 10  | OA2OUT/AD2AN1/CMP2A/ <b>RP17</b> /INT0/RB0                         | 24  | TDO/ <b>RP51</b> /PWM1H/IOMD4/RD2                |
| 11  | TMS/OA2IN-/AD1AN4/AD2ANN1/ <b>RP18</b> /RB1 <sup>(4)</sup>         | 25  | TDI/ <b>RP52</b> /PWM1L/IOMD5/RD3                |
| 12  | OA2IN+/AD2AN4/CMP2B/ <b>RP19</b> /RB2                              | 26  | V <sub>SS</sub>                                  |
| 13  | PGD1/AD1AN5/CMP1C/ISRC0/IBIAS0/ <b>RP20</b> /SDA1/RB3              | 27  | V <sub>DD</sub>                                  |
| 14  | PGC1/AD2AN5/CMP2C/ISRC1/IBIAS1/ <b>RP21</b> /SCL1/RB4              | 28  | MCLR                                             |

**Note:**

1. **RP<sub>n</sub>** represents remappable peripheral functions.
2. This pin has 8x drive strength.
3. Unless otherwise stated, pins are 4x drive strength. Refer to Electrical Specifications for current drive strength details.
4. A pull-up resistor is connected to this pin when device is erased (JTAG enabled) and during programming.

## Pin Diagrams

Figure 3. 36-Pin VQFN

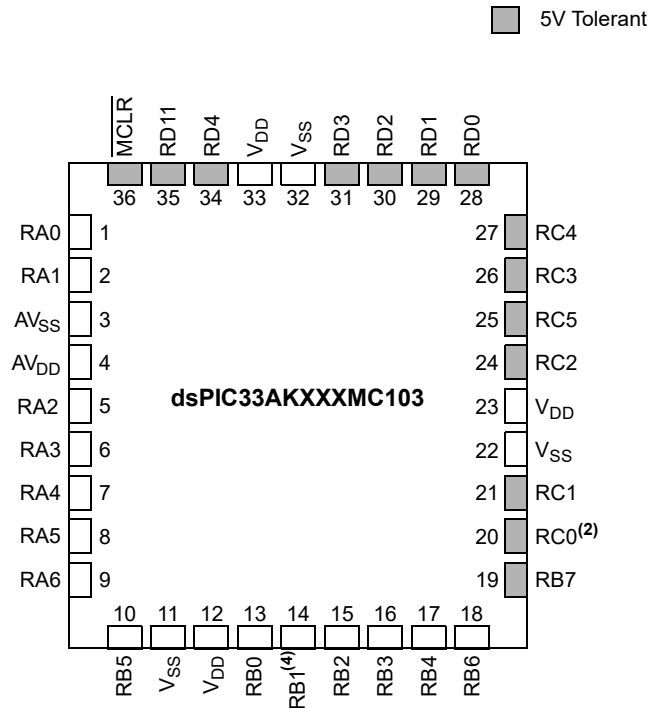


Table 4. 36-Pin VQFN Complete Pin Function Descriptions<sup>(1,3)</sup>

| Pin | Function                                                               | Pin | Function                                         |
|-----|------------------------------------------------------------------------|-----|--------------------------------------------------|
| 1   | PGD2/AD2AN6/CMP3C/ISRC2/IBIAS2/ <b>RP1</b> /SDA2/IOMF2/RA0             | 19  | AD2ANN2/AD2AN8/ <b>RP24</b> /IOMF0/RB7           |
| 2   | PGC2/DACOUT1/AD1AN7/AD2AN3/CMP1D/CMP2D/<br>CMP3D/ <b>RP2</b> /SCL2/RA1 | 20  | OSCO/CLKO/ <b>RP33</b> /IOMF5/RC0 <sup>(2)</sup> |
| 3   | AV <sub>SS</sub>                                                       | 21  | OSCI/CLKI/ <b>RP34</b> /IOMF6/RC1                |
| 4   | AV <sub>DD</sub>                                                       | 22  | V <sub>SS</sub>                                  |
| 5   | OA1OUT/AD1AN0/CMP1A/ <b>RP3</b> /RA2                                   | 23  | V <sub>DD</sub>                                  |
| 6   | OA1IN-/AD1ANN1/AD2AN0/ <b>RP4</b> /RA3                                 | 24  | PGC3/ <b>RP35</b> /PWM4H/RC2                     |
| 7   | OA1IN+/AD1AN1/CMP1B/ <b>RP5</b> /RA4                                   | 25  | <b>RP38</b> /PWM4L/RC5                           |
| 8   | OA3OUT/AD1AN3/CMP3A/ <b>RP6</b> /RA5                                   | 26  | PGD3/ <b>RP36</b> /PWM3H/IOMD0/RC3               |
| 9   | OA3IN-/AD1AN2/ <b>RP7</b> /RA6                                         | 27  | <b>RP37</b> /PWM3L/IOMD1/RC4                     |
| 10  | OA3IN+/AD2AN2/CMP3B/ <b>RP22</b> /RB5                                  | 28  | <b>RP49</b> /PWM2H/IOMD2/RD0                     |
| 11  | V <sub>SS</sub>                                                        | 29  | TCK/ <b>RP50</b> /PWM2L/IOMD3/RD1                |
| 12  | V <sub>DD</sub>                                                        | 30  | TDO/ <b>RP51</b> /PWM1H/IOMD4/RD2                |
| 13  | OA2OUT/AD2AN1/CMP2A/ <b>RP17</b> /INT0/RB0                             | 31  | TDI/ <b>RP52</b> /PWM1L/IOMD5/RD3                |
| 14  | TMS/OA2IN-/AD1AN4/AD2ANN1/ <b>RP18</b> /RB1 <sup>(4)</sup>             | 32  | V <sub>SS</sub>                                  |
| 15  | OA2IN+/AD2AN4/CMP2B/ <b>RP19</b> /RB2                                  | 33  | V <sub>DD</sub>                                  |
| 16  | PGD1/AD1AN5/CMP1C/ISRC0/IBIAS0/ <b>RP20</b> /SDA1/RB3                  | 34  | <b>RP53</b> /PCI22/RD4                           |
| 17  | PGC1/AD2AN5/CMP2C/ISRC1/IBIAS1/ <b>RP21</b> /SCL1/RB4                  | 35  | <b>RP60</b> /RD11                                |
| 18  | AD1ANN2/AD1AN8/ <b>RP23</b> /RB6                                       | 36  | MCLR                                             |

**Notes:**

- RPn** represents remappable peripheral functions.
- This pin has 8x drive strength.
- Unless otherwise stated, pins are 4x drive strength. Refer to Electrical Specifications for current drive strength details.
- A pull-up resistor is connected to this pin when device is erased (JTAG enabled) and during programming.

## Pin Diagrams

Figure 4. 48-Pin VQFN, TQFP

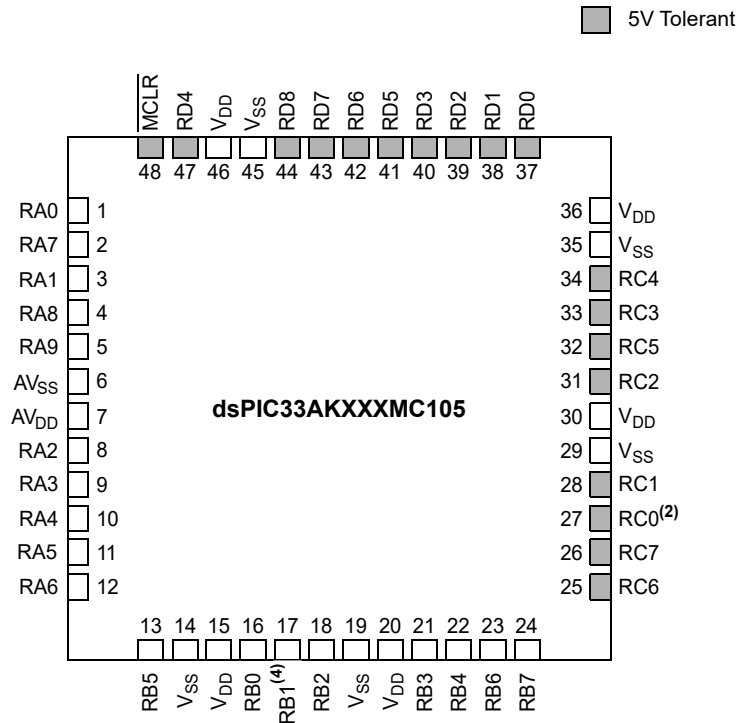


Table 5. 48-Pin VQFN, TQFP Complete Pin Function Descriptions<sup>(1,3)</sup>

| Pin | Function                                                               | Pin | Function                                         |
|-----|------------------------------------------------------------------------|-----|--------------------------------------------------|
| 1   | PGD2/AD2AN6/CMP3C/ISRC2/IBIAS2/ <b>RP1</b> /SDA2/IOMF2/RA0             | 25  | <b>RP39</b> /RC6                                 |
| 2   | AD1AN6/ <b>RP8</b> /IOMF1/RA7                                          | 26  | <b>RP40</b> /RC7                                 |
| 3   | PGC2/DACOUT1/AD1AN7/AD2AN3/CMP1D/CMP2D/<br>CMP3D/ <b>RP2</b> /SCL2/RA1 | 27  | OSCO/CLKO/ <b>RP33</b> /IOMF5/RC0 <sup>(2)</sup> |
| 4   | AD2AN9/ISRC3/IBIAS3/ <b>RP9</b> /RA8                                   | 28  | OSCI/CLKI/ <b>RP34</b> /IOMF6/RC1                |
| 5   | AD1ANN3/AD1AN9/ <b>RP10</b> /RA9                                       | 29  | V <sub>SS</sub>                                  |
| 6   | AV <sub>SS</sub>                                                       | 30  | V <sub>DD</sub>                                  |
| 7   | AV <sub>DD</sub>                                                       | 31  | PGC3/ <b>RP35</b> /PWM4H/RC2                     |
| 8   | OA1OUT/AD1AN0/CMP1A/ <b>RP3</b> /RA2                                   | 32  | <b>RP38</b> /PWM4L/RC5                           |
| 9   | OA1IN-/AD1ANN1/AD2AN0/ <b>RP4</b> /RA3                                 | 33  | PGD3/ <b>RP36</b> /PWM3H/IOMD0/RC3               |
| 10  | OA1IN+/AD1AN1/CMP1B/ <b>RP5</b> /RA4                                   | 34  | <b>RP37</b> /PWM3L/IOMD1/RC4                     |
| 11  | OA3OUT/AD1AN3/CMP3A/ <b>RP6</b> /RA5                                   | 35  | V <sub>SS</sub>                                  |
| 12  | OA3IN-/AD1AN2/ <b>RP7</b> /RA6                                         | 36  | V <sub>DD</sub>                                  |
| 13  | OA3IN+/AD2AN2/CMP3B/ <b>RP22</b> /RB5                                  | 37  | <b>RP49</b> /PWM2H/IOMD2/RD0                     |
| 14  | V <sub>SS</sub>                                                        | 38  | TCK/ <b>RP50</b> /PWM2L/IOMD3/RD1                |
| 15  | V <sub>DD</sub>                                                        | 39  | TDO/ <b>RP51</b> /PWM1H/IOMD4/RD2                |
| 16  | OA2OUT/AD2AN1/CMP2A/ <b>RP17</b> /INT0/RB0                             | 40  | TDI/ <b>RP52</b> /PWM1L/IOMD5/RD3                |
| 17  | TMS/OA2IN-/AD1AN4/AD2ANN1/ <b>RP18</b> /RB1 <sup>(4)</sup>             | 41  | <b>RP54</b> /ASCL1/RD5                           |
| 18  | OA2IN+/AD2AN4/CMP2B/ <b>RP19</b> /RB2                                  | 42  | <b>RP55</b> /ASDA1/RD6                           |
| 19  | V <sub>SS</sub>                                                        | 43  | <b>RP56</b> /ASCL2/IOMD7/IOMF4/RD7               |
| 20  | V <sub>DD</sub>                                                        | 44  | <b>RP57</b> /ASDA2/IOMD6/IOMF3/RD8               |
| 21  | PGD1/AN1P5/CMP1C/ISRC0/IBIAS0/ <b>RP20</b> /SDA1/RB3                   | 45  | V <sub>SS</sub>                                  |
| 22  | PGC1/AD2AN5/CMP2C/ISRC1/IBIAS1/ <b>RP21</b> /SCL1/RB4                  | 46  | V <sub>DD</sub>                                  |
| 23  | AD1ANN2/AD1AN8/ <b>RP23</b> /RB6                                       | 47  | <b>RP53</b> /PCI22/RD4                           |
| 24  | AD2ANN2/AD2AN8/ <b>RP24</b> /IOMF0/RB7                                 | 48  | MCLR                                             |

.....continued

| Pin | Function | Pin | Function |
|-----|----------|-----|----------|
|-----|----------|-----|----------|

**Note:**

1. **RPn** represents remappable peripheral functions.
2. This pin has 8x drive strength.
3. Unless otherwise stated, pins are 4x drive strength. Refer to Electrical Specifications for current drive strength details.
4. A pull-up resistor is connected to this pin when device is erased (JTAG enabled) and during programming.

## Pin Diagrams

Figure 5. 64-Pin VQFN, TQFP

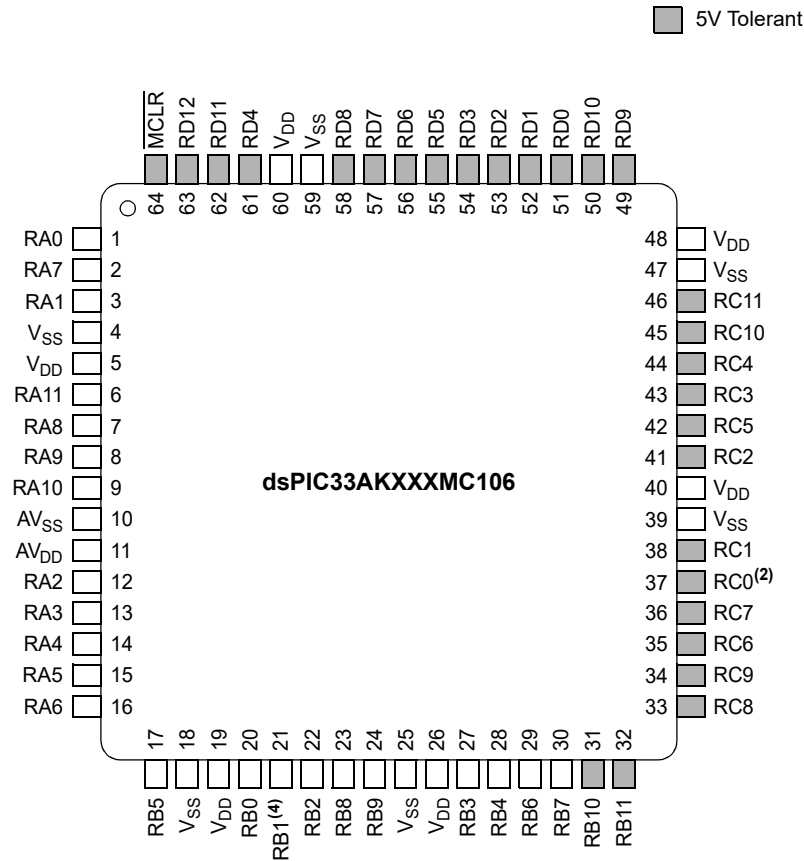


Table 6. 64-Pin VQFN, TQFP Complete Pin Function Descriptions<sup>(1,3)</sup>

| Pin | Function                                                               | Pin | Function                                         |
|-----|------------------------------------------------------------------------|-----|--------------------------------------------------|
| 1   | PGD2/AD2AN6/CMP3C/ISRC2/IIBIAS2/ <b>RP1</b> /SDA2/IOMF2/RA0            | 33  | <b>RP41</b> /IOMD11/IOMF11/PCI20/RC8             |
| 2   | AD1AN6/ <b>RP8</b> /IOMF1/RA7                                          | 34  | <b>RP42</b> /IOMD10/SDO2/IOMF10/PCI19/RC9        |
| 3   | PGC2/DACOUT1/AD1AN7/AD2AN3/CMP1D/CMP2D/<br>CMP3D/ <b>RP2</b> /SCL2/RA1 | 35  | <b>RP39</b> /RC6                                 |
| 4   | V <sub>SS</sub>                                                        | 36  | <b>RP40</b> /RC7                                 |
| 5   | V <sub>DD</sub>                                                        | 37  | OSCO/CLKO/ <b>RP33</b> /IOMF5/RC0 <sup>(2)</sup> |
| 6   | AD1AN10/ <b>RP12</b> /RA11                                             | 38  | OSCI/CLKI/ <b>RP34</b> /IOMF6/RC1                |
| 7   | AD2AN9/ISRC3/IIBIAS3/ <b>RP9</b> /RA8                                  | 39  | V <sub>SS</sub>                                  |
| 8   | AD1ANN3/AD1AN9/ <b>RP10</b> /RA9                                       | 40  | V <sub>DD</sub>                                  |
| 9   | AD2ANN3/AD2AN7/ <b>RP11</b> /RA10                                      | 41  | PGC3/ <b>RP35</b> /PWM4H/RC2                     |
| 10  | AV <sub>SS</sub>                                                       | 42  | <b>RP38</b> /PWM4L/RC5                           |
| 11  | AV <sub>DD</sub>                                                       | 43  | PGD3/ <b>RP36</b> /PWM3H/IOMD0/RC3               |
| 12  | OA1OUT/AD1AN0/CMP1A/ <b>RP3</b> /RA2                                   | 44  | <b>RP37</b> /PWM3L/IOMD1/RC4                     |
| 13  | OA1IN-/AD1ANN1/AD2AN0/ <b>RP4</b> /RA3                                 | 45  | <b>RP43</b> /IOMD9/IOMF9/RC10                    |
| 14  | OA1IN+/AD1AN1/CMP1B/ <b>RP5</b> /RA4                                   | 46  | <b>RP44</b> /IOMD8/IOMF8/RC11                    |
| 15  | OA3OUT/AD1AN3/CMP3A/ <b>RP6</b> /RA5                                   | 47  | V <sub>SS</sub>                                  |
| 16  | OA3IN-/AD1AN2/ <b>RP7</b> /RA6                                         | 48  | V <sub>DD</sub>                                  |
| 17  | OA3IN+/AD2AN2/CMP3B/ <b>RP22</b> /RB5                                  | 49  | <b>RP58</b> /IOMF7/RD9                           |
| 18  | V <sub>SS</sub>                                                        | 50  | <b>RP59</b> /RD10                                |
| 19  | V <sub>DD</sub>                                                        | 51  | <b>RP49</b> /PWM2H/IOMD2/RD0                     |
| 20  | OA2OUT/AD2AN1/CMP2A/ <b>RP17</b> /INT0/RB0                             | 52  | TCK/ <b>RP50</b> /PWM2L/IOMD3/RD1                |

.....continued

| Pin | Function                                                   | Pin | Function                           |
|-----|------------------------------------------------------------|-----|------------------------------------|
| 21  | TMS/OA2IN-/AD1AN4/AD2ANN1/ <b>RP18</b> /RB1 <sup>(4)</sup> | 53  | TDO/ <b>RP51</b> /PWM1H/IOMD4/RD2  |
| 22  | OA2IN+/AD2AN4/CMP2B/ <b>RP19</b> /RB2                      | 54  | TDI/ <b>RP52</b> /PWM1L/IOMD5/RD3  |
| 23  | AD1AN11/ <b>RP25</b> /RB8                                  | 55  | <b>RP54</b> /ASCL1/RD5             |
| 24  | AD2AN10/ <b>RP26</b> /RB9                                  | 56  | <b>RP55</b> /ASDA1/RD6             |
| 25  | V <sub>SS</sub>                                            | 57  | <b>RP56</b> /ASCL2/IOMD7/IOMF4/RD7 |
| 26  | V <sub>DD</sub>                                            | 58  | <b>RP57</b> /ASDA2/IOMD6/IOMF3/RD8 |
| 27  | PGD1/AD1AN5/CMP1C/ISRC0/IBIAS0/ <b>RP20</b> /SDA1/RB3      | 59  | V <sub>SS</sub>                    |
| 28  | PGC1/AD2AN5/CMP2C/ISRC1/IBIAS1/ <b>RP21</b> /SCL1/RB4      | 60  | V <sub>DD</sub>                    |
| 29  | AD1ANN2/AD1AN8/ <b>RP23</b> /RB6                           | 61  | <b>RP53</b> /PCI22/RD4             |
| 30  | AD2ANN2/AD2AN8/ <b>RP24</b> /IOMF0/RB7                     | 62  | <b>RP60</b> /RD11                  |
| 31  | <b>RP27</b> /SCK2/RB10                                     | 63  | <b>RP61</b> /PCI21/RD12            |
| 32  | <b>RP28</b> /SDI2/RB11                                     | 64  | MCLR                               |

**Note:**

1. **RPn** represents remappable peripheral functions.
2. This pin has 8x drive strength.
3. Unless otherwise stated, pins are 4x drive strength. Refer to Electrical Specifications for current drive strength details.
4. A pull-up resistor is connected to this pin when device is erased (JTAG enabled) and during programming.

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