Automotive DDR2 SDRAM Data Sheet Addendum

MT47H128M8 – 16 Meg x 8 x 8 banks
MT47H64M16 – 8 Meg x 16 x 8 banks

Features

- This addendum provides information to add Automotive Ultra-high Temperature (AUT) option[2] for the data sheet. This addendum does not provide detailed information about the device. Refer to the full data sheet for a complete description of device functionality, operating modes, and specifications for the same Micron part number products.
- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- RoHS-compliant
- Supports JEDEC clock jitter specification
- PPAP submission
- 8D response time

Options[1]	Marking
• Configuration	
– 128 Meg x 8 (16 Meg x 8 x 8 banks)	128M8
– 64 Meg x 16 (8 Meg x 16 x 8 banks)	64M16
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (8mm x 12.5mm)	NF
• FBGA package (Pb-free) – x8	
– 60-ball FBGA (8mm x 10mm)	SH
• Timing – cycle time	
– 2.5ns @ CL = 5 (DDR2-800)	-25E
• Special option	
– Standard	None
– Automotive grade	A
• Operating temperature	
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
– Automotive (–40°C ≤ T_C ≤ +105°C)	AT
– Ultra-high (–40°C ≤ T_C ≤ +125°C)	UT
• Revision	:M

Notes:
1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.
2. UT option use based on automotive usage model. Please contact Micron sales representative if you have questions.

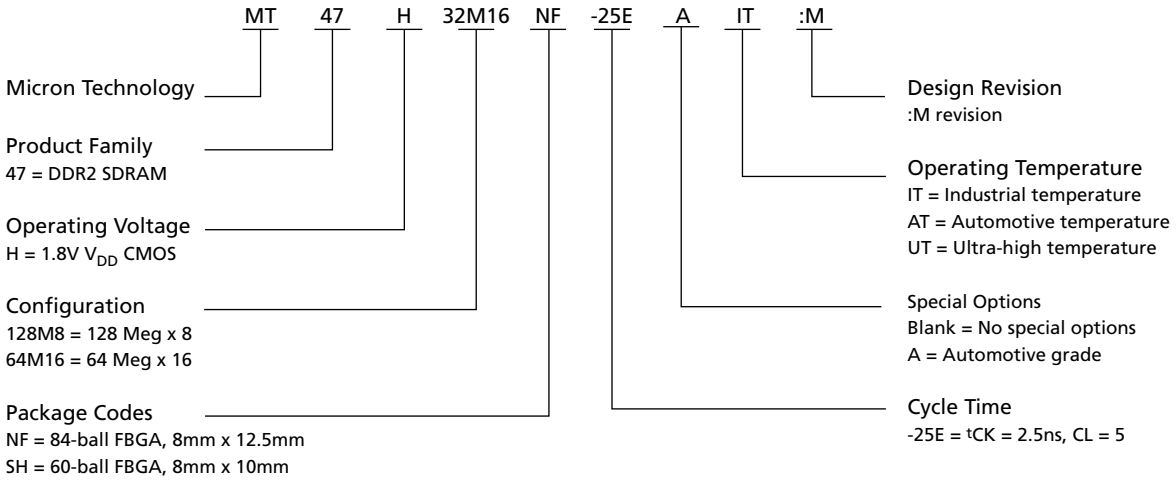
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)				^{t}RC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	
-25E	400	533	800	800	55

Table 2: Addressing

Parameter	128 Meg x 8	64 Meg x 16
Configuration	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K
Row address	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[2:0] (8)	BA[2:0] (8)
Column address	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 1Gb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available in all packages.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

Important Notes and Warnings

Micron Technology, Inc. ("Micron") reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions. This document supersedes and replaces all information supplied prior to the publication hereof. You may not rely on any information set forth in this document if you obtain the product described herein from any unauthorized distributor or other source not authorized by Micron.

Automotive Applications. Products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets. Distributor and customer/distributor shall assume the sole risk and liability for and shall indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of non-automotive-grade products in automotive applications. Customer/distributor shall ensure that the terms and conditions of sale between customer/distributor and any customer of distributor/customer (1) state that Micron products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets and (2) require such customer of distributor/customer to indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting from any use of non-automotive-grade products in automotive applications.

Critical Applications. Products are not authorized for use in applications in which failure of the Micron component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("Critical Applications"). Customer must protect against death, personal injury, and severe property and environmental damage by incorporating safety design measures into customer's applications to ensure that failure of the Micron component will not result in such harms. Should customer or distributor purchase, use, or sell any Micron component for any critical application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such critical application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.

Customer Responsibility. Customers are responsible for the design, manufacture, and operation of their systems, applications, and products using Micron products. ALL SEMICONDUCTOR PRODUCTS HAVE INHERENT FAILURE RATES AND LIMITED USEFUL LIVES. IT IS THE CUSTOMER'S SOLE RESPONSIBILITY TO DETERMINE WHETHER THE MICRON PRODUCT IS SUITABLE AND FIT FOR THE CUSTOMER'S SYSTEM, APPLICATION, OR PRODUCT. Customers must ensure that adequate design, manufacturing, and operating safeguards are included in customer's applications and products to eliminate the risk that personal injury, death, or severe property or environmental damages will result from failure of any semiconductor component.

Limited Warranty. In no event shall Micron be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Micron's duly authorized representative.

Functional Description

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR2 SDRAM enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Automotive Industrial Temperature (AIT)

The industrial temperature (AIT) option, if offered, the case temperature cannot be less than –40°C or greater than +95°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, the input/output impedance, and I_{DD} values must be derated when T_C is < 0°C or > +85°C.

Automotive-grade Automotive Temperature (AAT)

The automotive-grade automotive temperature (AAT) option, if offered, the case temperature cannot be less than –40°C or greater than +105°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, the input/output impedance, and I_{DD} values must be derated when T_C is < 0°C or > +85°C.

Automotive Ultra-high Temperature (AUT)

The automotive ultra-high temperature (AUT) option, if offered, the case temperature cannot be less than –40°C or greater than +125°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature auto refresh mode. When Tc > +105C, the refresh rate must be increased to 8X. Self refresh mode is not available for Tc >+105°C. . Additionally, ODT resistance, the input/output impedance, and I_{DD} values must be derated when T_C is < 0°C or > +85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor
  - Connect UDQS# to V_{DD} via 1kΩ* resistor
  - Connect UDM to V_{DD} via 1kΩ* resistor
  - Connect DQ[15:8] individually to either V_{SS} or V_{DD} via 1kΩ* resistors, or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Electrical Specifications – Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 3: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–1.0	2.3	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.5	2.3	V	1, 2
V_{DDL} supply voltage relative to V_{SSL}	V_{DDL}	–0.5	2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V	3
Input leakage current; any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V	I_I	–5	5	µA	
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled	I_{OZ}	–5	5	µA	
V_{REF} leakage current; V_{REF} = Valid V_{REF} level	I_{VREF}	–2	2	µA	

Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times; this is not required when power is ramping down.
2. V_{REF} ≤ 0.6 × V_{DDQ}; however, V_{REF} may be ≥ V_{DDQ} provided that V_{REF} ≤ 300mV.
3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 4 (page 7), be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 5 (page 7) for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 5. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

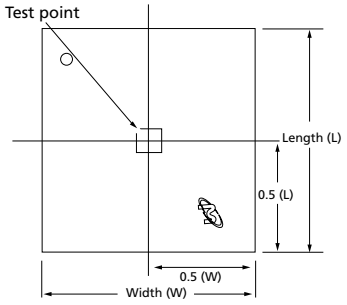
The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Table 4: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	–55	150	°C	1
Operating temperature: commercial (CT)	T_C	0	85	°C	2, 3
Operating temperature: industrial (IT)	T_C	–40	95	°C	2, 3,
Operating temperature: automotive (AT)	T_C	–40	105	°C	2, 3,
Operating temperature: ultra-high (UT)	T_C	–40	125	°C	2,3,4

Notes:
1. MAX storage case temperature T_{STG} is measured in the center of the package, as shown in Figure 2. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
2. MAX operating case temperature T_C is measured in the center of the package, as shown in Figure 2.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Ultra-high temperature use based on automotive usage model. Please contact Micron sales representative if you have questions.

Figure 2: Example Temperature Test Point Location



Lmm x Wmm FBGA

Table 5: Thermal Impedance

Die Revision	Package	Substrate (pcb)	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
M[1]	60-ball	Low Conductivity	85.4	70.6	64.5	42.8	11.7
		High Conductivity	63.2	56.1	52.8		
	84-ball	Low Conductivity	80.8	67.0	61.6	44.7	11.7
		High Conductivity	59.7	53.3	50.7		

Note:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Electrical Specifications – I_{DD} Parameters

I_{DD} Specifications and Conditions

Table 6: General I_{DD} Parameters

I_{DD} Parameters	-25E	Units
CL (I_{DD})	5	^{t}CK
^{t}RCD (I_{DD})	12.5	ns
^{t}RC (I_{DD})	57.5	ns
^{t}RRD (I_{DD}) - x8 (1KB)	7.5	ns
^{t}RRD (I_{DD}) - x16 (2KB)	10	ns
^{t}CK (I_{DD})	2.5	ns
^{t}RAS MIN (I_{DD})	45	ns
^{t}RAS MAX (I_{DD})	70,000	ns
^{t}RP (I_{DD})	12.5	ns
^{t}RFC (I_{DD} - 256Mb)	75	ns
^{t}RFC (I_{DD} - 512Mb)	105	ns
^{t}RFC (I_{DD} - 1Gb)	127.5	ns
^{t}RFC (I_{DD} - 2Gb)	197.5	ns
^{t}FAW (I_{DD}) - x8 (1KB)	Defined by pattern in Table 7 (page 8)	ns
^{t}FAW (I_{DD}) - x16 (2KB)	Defined by pattern in Table 7 (page 8)	ns

I_{DD7} Conditions

The detailed timings are shown below for I_{DD7}. Where general I_{DD} parameters in Table 6 (page 8) conflict with pattern requirements of Table 7, then Table 7 requirements take precedence.

Table 7: I_{DD7} Timing Patterns (8-Bank Interleave READ Operation)

Speed Grade	I_{DD7} Timing Patterns
Timing patterns for 8-bank x4/x8 devices	
-25E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
Timing patterns for 8-bank x16 devices	
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D

Notes:
1. A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at ^{t}RC (I_{DD}) without violating ^{t}RRD (I_{DD}) using a BL = 4.
3. Control and address bus inputs are stable during deselects.

Table 8: DDR2 I_{DD} Specifications and Conditions (Die Revision M)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-25E	Units
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x8	65	mA
		x16	80	
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}), $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x8	75	mA
		x16	95	
Precharge power-down current: All banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x8, x16	10	mA
Precharge quiet standby current: All banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x8	24	mA
		x16	26	
Precharge standby current: All banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x8	28	mA
		x16	30	
Active power-down current: All banks open; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast exit MR12 = 0	30	mA
	I_{DD3Ps}	Slow exit MR12 = 1	20	
Active standby current: All banks open; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x8	33	mA
		x16	38	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x8	125	mA
		x16	160	
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}	x8	120	mA
		x16	150	
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; REFRESH command at every $^{t}RFC (I_{DD})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}	x8	155	mA
		x16	160	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}	x8, x16	7	mA

Table 8: DDR2 I_{DD} Specifications and Conditions (Die Revision M) (Continued)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-25E	Units
Operating bank interleave read current: All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = ^{t}RCD (I_{DD}) - 1 × ^{t}CK (I_{DD}); ^{t}CK = ^{t}CK (I_{DD}), ^{t}RC = ^{t}RC (I_{DD}), ^{t}RRD = ^{t}RRD (I_{DD}), ^{t}RCD = ^{t}RCD (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions for details	I_{DD7}	x8	210	mA
		x16	260	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C.
2. V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{DDL} = +1.8V ±0.1V, V_{REF} = V_{DDQ}/2.
3. I_{DD} parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. I_{DD} values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for I_{DD} conditions:

   LOW $V_{IN} \le V_{IL(AC)max}$

   HIGH $V_{IN} \ge V_{IH(AC)min}$

   Stable Inputs stable at a HIGH or LOW level

   Floating Inputs at $V_{REF} = V_{DDQ}/2$

   Switching Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals

   Switching Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes
6. I_{DD1}, I_{DD4R}, and I_{DD7} require A12 in EMR to be enabled during testing.
7. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option and AT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:

   When T_C ≤ 0°C I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%

   When T_C ≥85°C I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5} must be derated by 2%; I_{DD2P} must be derated by 20%; $I_{DD3P(SLOW)}$ must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2X refresh option is still enabled)

   When T_C ≥105°C 8X refresh is required, self-refresh mode is not available.

Table 9: AC Operating Specifications and Conditions

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table;
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-25E			
Parameter		Symbol	Min	Max	Units	Notes
Clock	Clock cycle time	CL = 6	^tCK (avg)	2.5	8.0	ns	6, 7, 8, 9
		CL = 5	^tCK (avg)	2.5	8.0		
		CL = 4	^tCK (avg)	3.75	8.0		
		CL = 3	^tCK (avg)	5.0	8.0		
	CK high-level width		^tCH (avg)	0.48	0.52	^tCK	10
	CK low-level width		^tCL (avg)	0.48	0.52	^tCK	
	Half clock period		^tHP	MIN = lesser of ^tCH and ^tCL MAX = n/a		ps	11
	Absolute ^tCK		^tCK (abs)	MIN = ^tCK (AVG) MIN + ^tJITper (MIN) MAX = ^tCK (AVG) MAX + ^tJITper (MAX)		ps	
	Absolute CK high-level width		^tCH (abs)	MIN = ^tCK (AVG) MIN × ^tCH (AVG) MIN + ^tJITdty (MIN) MAX = ^tCK (AVG) MAX × ^tCH (AVG) MAX + ^tJITdty (MAX)		ps	
	Absolute CK low-level width		^tCL (abs)	MIN = ^tCK (AVG) MIN × ^tCL (AVG) MIN + ^tJITdty (MIN) MAX = ^tCK (AVG) MAX × ^tCL (AVG) MAX + ^tJITdty (MAX)		ps	
Clock Jitter	Period jitter		^tJITper	–100	100	ps	12
	Half period		^tJITdty	–100	100	ps	13
	Cycle to cycle		^tJITcc	200		ps	14
	Cumulative error, 2 cycles		$^tERR_{2per}$	–150	150	ps	15
	Cumulative error, 3 cycles		$^tERR_{3per}$	–175	175	ps	15
	Cumulative error, 4 cycles		$^tERR_{4per}$	–200	200	ps	15
	Cumulative error, 5 cycles		$^tERR_{5per}$	–200	200	ps	15, 16
	Cumulative error, 6–10 cycles		$^tERR_{6-10per}$	–300	300	ps	15, 16
	Cumulative error, 11–50 cycles		$^tERR_{11-50per}$	–450	450	ps	15
Data Strobe-Out	DQS output access time from CK/CK#		^tDQSCK	–350	350	ps	19
	DQS read preamble		^tRPRE	MIN = 0.9 × ^tCK MAX = 1.1 × ^tCK		^tCK	17, 18, 19
	DQS read postamble		^tRPST	MIN = 0.4 × ^tCK MAX = 0.6 × ^tCK		^tCK	17, 18, 19, 20
	CK/CK# to DQS Low-Z		$^tLZ_1$	MIN = ^tAC (MIN) MAX = ^tAC (MAX)		ps	19, 21, 22

Table 9: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table;
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-25E			
	Parameter	Symbol	Min	Max	Units	Notes
Data Strobe-In	DQS rising edge to CK rising edge	tDQSS	MIN = –0.25 × tCK MAX = 0.25 × tCK		tCK	18
	DQS input-high pulse width	tDQSH	MIN = 0.35 × tCK MAX = n/a		tCK	18
	DQS input-low pulse width	tDQSL	MIN = 0.35 × tCK MAX = n/a		tCK	18
	DQS falling to CK rising: set-up time	tDSS	MIN = 0.2 × tCK MAX = n/a		tCK	18
	DQS falling from CK rising: hold time	tDSH	MIN = 0.2 × tCK MAX = n/a		tCK	18
	Write preamble setup time	tWPRES	MIN = 0 MAX = n/a		ps	23, 24
	DQS write preamble	tWPRE	MIN = 0.35 × tCK MAX = n/a		tCK	18
	DQS write postamble	tWPST	MIN = 0.4 × tCK MAX = 0.6 × tCK		tCK	18, 25
	WRITE command to first DQS transition	–	MIN = WL - tDQSS MAX = WL + tDQSS		tCK	
Data-Out	DQ output access time from CK/CK#	tAC	–400	400	ps	19
	DQS–DQ skew, DQS to last DQ valid, per group, per access	tDQSQ	–	200	ps	26, 27
	DQ hold from next DQS strobe	tQHS	–	300	ps	28
	DQ–DQS hold, DQS to first DQ not valid	tQH	MIN = tHP - tQHS MAX = n/a		ps	26, 27, 28
	CK/CK# to DQ, DQS High-Z	tHZ	MIN = n/a MAX = tAC (MAX)		ps	19, 21, 29
	CK/CK# to DQ Low-Z	tLZ_2	MIN = 2 × tAC (MIN) MAX = tAC (MAX)		ps	19, 21, 22
	Data valid output window	DVW	MIN = tQH - tDQSQ MAX = n/a		ns	26, 27

Table 9: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table;
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-25E			
Parameter			Symbol	Min	Max	Units	Notes
Data-In	DQ and DM input setup time to DQS		tDSb	50	–	ps	26, 30, 31
	DQ and DM input hold time to DQS		tDHb	125	–	ps	26, 30, 31
	DQ and DM input setup time to DQS		tDSa	250	–	ps	26, 30, 31
	DQ and DM input hold time to DQS		tDHa	250	–	ps	26, 30, 31
	DQ and DM input pulse width		tDIPW	MIN = 0.35 × tCK MAX = n/a		tCK	18, 32
Command and Address	Input setup time		tISb	175	–	ps	31, 33
	Input hold time		tIHb	250	–	ps	31, 33
	Input setup time		tISa	375	–	ps	31, 33
	Input hold time		tIHa	375	–	ps	31, 33
	Input pulse width		tIPW	0.6	–	tCK	18, 32
	ACTIVATE-to-ACTIVATE delay, same bank		tRC	55	–	ns	18, 34, 51
	ACTIVATE-to-READ or WRITE delay		tRCD	12.5	–	ns	18
	ACTIVATE-to-PRECHARGE delay		tRAS	45	70K	ns	18, 34, 35
	PRECHARGE period		tRP	12.5	–	ns	18, 36
	PRECHARGE ALL period	<1Gb	tRPA	12.5	–	ns	18, 36
		≥1Gb	tRPA	15	–	ns	18, 36
	ACTIVATE-to-ACTIVATE delay different bank	x8	tRRD	7.5	–	ns	18, 37
		x16	tRRD	10	–	ns	18, 37
	4-bank activate period (≥1Gb)	x8	tFAW	35	–	ns	18, 38
		x16	tFAW	45	–	ns	18, 38

Table 9: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table;
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-25E			
Parameter		Symbol	Min	Max	Units	Notes
Command and Address	Internal READ-to-PRECHARGE delay		^{t}RTP	7.5	–	ns	18, 37, 39
	CAS#-to-CAS# delay		^{t}CCD	2	–	^{t}CK	18
	Write recovery time		^{t}WR	15	–	ns	18, 37
	Write AP recovery + precharge time		^{t}DAL	^{t}WR + ^{t}RP	–	ns	40
	Internal WRITE-to-READ delay		^{t}WTR	7.5	–	ns	18, 37
	LOAD MODE cycle time		^{t}MRD	2	–	^{t}CK	18
Refresh	REFRESH-to-ACTIVATE or to -REFRESH interval	256Mb	^{t}RFC	75	–	ns	18, 41
		512Mb		105	–		
		1Gb		127.5	–		
		2Gb		195	–		
	Average periodic refresh (commercial)		^{t}REFI	–	7.8	µs	18, 41
	Average periodic refresh (industrial)		^{t}REFI$_{IT}$	–	3.9	µs	18, 41
	Average periodic refresh (automotive)		^{t}REFI$_{AT}$	–	3.9	µs	18, 41
	Average periodic refresh (automotive)		^{t}REFI$_{UT}$	–	0.975	µs	18, 41
	CKE LOW to CK, CK# uncertainty		^{t}DELAY	MIN limit = ^{t}IS + ^{t}CK + ^{t}IH MAX limit = n/a		ns	42
Self Refresh	Exit SELF REFRESH to non-READ command		^{t}XSNR	MIN limit = ^{t}RFC (MIN) + 10 MAX limit = n/a		ns	52
	Exit SELF REFRESH to READ command		^{t}XSRD	MIN limit = 200 MAX limit = n/a		^{t}CK	18, 52
	Exit SELF REFRESH timing reference		^{t}ISXR	MIN limit = ^{t}IS MAX limit = n/a		ps	33, 43, 52

Table 9: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table;
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-25E			
Parameter			Symbol	Min	Max	Units	Notes
Power-Down	Exit active power-down to READ command	MR12 = 0	tXARD	2	–	tCK	18
		MR12 = 1		8 - AL	–	tCK	18
	Exit precharge power-down and active power-down to any nonREAD command		tXP	2	–	tCK	18
	CKE MIN HIGH/LOW time		tCKE	MIN = 3 MAX = n/a		tCK	18, 44
ODT	ODT to power-down entry latency		tANPD	3	–	tCK	18
	ODT power-down exit latency		tAXPD	8	–	tCK	18
	ODT turn-on delay		tAOND	2		tCK	18
	ODT turn-off delay		tAOFD	2.5		tCK	18, 45
	ODT turn-on		tAON	MIN = tAC (MIN) MAX = tAC (MAX) + 600		ps	19, 46
	ODT turn-off		tAOF	MIN = tAC (MIN) MAX = tAC (MAX) + 600		ps	47, 48
	ODT turn-on (power-down mode)		tAONPD	MIN = tAC (MIN) + 2000 MAX = 2 × tCK + tAC (MAX) + 1000		ps	49
	ODT turn-off (power-down mode)		tAOFPD	MIN = tAC (MIN) + 2000 MAX = 2.5 × tCK + tAC (MAX) + 1000		ps	
	ODT enable from MRS command		tMOD	MIN = 12 MAX = n/a		ns	18, 50

Notes:
1. All voltages are referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the operation of the device are warranted for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Outputs measured with equivalent load (see Figure 2).
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment, and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0 V/ns for signals in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$. Slew rates other than 1.0 V/ns may require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
7. Operating frequency is only allowed to change during self refresh mode (see Figure 1), precharge power-down mode, or system reset condition (see Reset). SSC allows for small deviations in operating frequency, provided the SSC guidelines are satisfied.
8. The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK (AVG) MIN is the smallest clock rate allowed (except for a deviation due to allowed clock jitter). Input clock jitter is allowed provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
9. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range 8–60 kHz with an additional one percent ^{t}CK (AVG); however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN or above ^{t}CK (AVG) MAX.
10. MIN (^{t}CL, ^{t}CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; ^{t}CH (AVG) and ^{t}CL (AVG) must be met with or without clock jitter and with or without duty cycle jitter. ^{t}CH (AVG) and ^{t}CL (AVG) are the average of any 200 consecutive CK falling edges. ^{t}CH limits may be exceeded if the duty cycle jitter is small enough that the absolute half period limits (^{t}CH [ABS], ^{t}CL [ABS]) are not violated.
11. ^{t}HP (MIN) is the lesser of ^{t}CL and ^{t}CH actually applied to the device CK and CK# inputs; thus, ^{t}HP (MIN) ≥ the lesser of ^{t}CL (ABS) MIN and ^{t}CH (ABS) MIN.
12. The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less those than noted in the table (DLL locked).
13. The half-period jitter (^{t}JITdty) applies to either the high pulse of clock or the low pulse of clock; however, the two cumulatively can not exceed ^{t}JITper.
14. The cycle-to-cycle jitter (^{t}JITcc) is the amount the clock period can deviate from one cycle to the next. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than those noted in the table (DLL locked).
15. The cumulative jitter error ($^{t}ERR_{nper}$), where *n* is 2, 3, 4, 5, 6–10, or 11–50 is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
16. JEDEC specifies using $^{t}ERR_{6–10per}$ when derating clock-related output timing (see notes 19 and 48). Micron requires less derating by allowing $^{t}ERR_{5per}$ to be used.
17. This parameter is not referenced to a specific voltage level but is specified when the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).
18. The inputs to the DRAM must be aligned to the associated clock, that is, the actual clock that latches it in. However, the input timing (in ns) references to the ^{t}CK (AVG) when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the ^{t}CK (AVG) rather than ^{t}CK: ^{t}IPW, ^{t}DIPW, ^{t}DQSS, ^{t}DQSH, ^{t}DQSL, ^{t}DSS, ^{t}DSH, ^{t}WPST, and ^{t}WPRE.
19. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}ERR_{5per}$ (MAX): ^{t}AC (MIN), ^{t}DQSCK (MIN), $^{t}LZ_{DQS}$ (MIN), $^{t}LZ_{DQ}$ (MIN), ^{t}AON (MIN); while the following parameters are required to be derated by subtracting $^{t}ERR_{5per}$ (MIN): ^{t}AC (MAX), ^{t}DQSCK (MAX), ^{t}HZ (MAX), $^{t}LZ_{DQS}$ (MAX), $^{t}LZ_{DQ}$ (MAX), ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX), is derated by subtracting ^{t}JITper (MIN). The parameter ^{t}RPST (MIN) is derated by subtracting ^{t}JITdty (MAX), while ^{t}RPST (MAX), is derated by subtracting ^{t}JITdty (MIN). Output timings that require $^{t}ERR_{5per}$ derating can be observed to have offsets relative to the clock; however, the total window will not degrade.
20. When DQS is used single-ended, the minimum limit is reduced by 100ps.

21. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
22. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
23. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
24. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
25. The intent of the "Don't Care" state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above $V_{IH[DC]min}$), then it must not transition LOW (below $V_{IH[DC]}$) prior to ^{t}DQSH (MIN).
26. Referenced to each output group: x8 = DQS with DQ[7:0]; x16 = LDQS with DQ[7:0]; and UDQS with DQ[15:8].
27. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
28. ^{t}QH = ^{t}HP - ^{t}QHS; the worst case ^{t}QH would be the lesser of ^{t}CL (ABS) MAX or ^{t}CH (ABS) MAX times ^{t}CK (ABS) MIN - ^{t}QHS. Minimizing the amount of ^{t}CH (AVG) offset and value of ^{t}JITdty will provide a larger ^{t}QH, which in turn will provide a larger valid data out window.
29. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
30. The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew rate of 2 V/ns (1 V/ns for each signal). There are two sets of values listed: $^{t}DS_a$, $^{t}DH_a$ and $^{t}DS_b$, $^{t}DH_b$. The $^{t}DS_a$, $^{t}DH_a$ values (for reference only) are equivalent to the baseline values of $^{t}DS_b$, $^{t}DH_b$ at V_{REF} when the slew rate is 2 V/ns, differentially. The baseline values, $^{t}DS_b$, $^{t}DH_b$, are the JEDEC-defined values, referenced from the logic trip points. $^{t}DS_b$ is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while $^{t}DH_b$ is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated by adding the values from Table 3 and Table 4. If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended and the baseline values must be derated using Table 5. Single-ended DQS data timing is referenced at DQS crossing V_{REF}. The correct timing values for a single-ended DQS strobe are listed in Table 6–Table 8 on Table 6, Table 7, and Table 8; listed values are already derated for slew rate variations and converted from baseline values to V_{REF} values.
31. V_{IL}/V_{IH} DDR2 overshoot/undershoot. See AC Overshoot/Undershoot Specification.
32. For each input signal—not the group collectively.
33. There are two sets of values listed for command/address: $^{t}IS_a$, $^{t}IH_a$ and $^{t}IS_b$, $^{t}IH_b$. The $^{t}IS_a$, $^{t}IH_a$ values (for reference only) are equivalent to the baseline values of $^{t}IS_b$, $^{t}IH_b$ at V_{REF} when the slew rate is 1 V/ns. The baseline values, $^{t}IS_b$, $^{t}IH_b$, are the JEDEC-defined values, referenced from the logic trip points. $^{t}IS_b$ is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while $^{t}IH_b$ is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal. If the command/address slew rate is not equal to 1 V/ns, then the baseline values must be derated by adding the values from Table 1 and Table 2.
34. This is applicable to READ cycles only. WRITE cycles generally require additional time due to ^{t}WR during auto precharge.
35. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied because ^{t}RAS lockout feature is supported in DDR2 SDRAM.

36. When a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks open. For 8-bank devices (≥1Gb), ^{t}RPA (MIN) = ^{t}RP (MIN) + ^{t}CK (AVG) (Table 9 (page 11) lists ^{t}RP [MIN] + ^{t}CK [AVG] MIN).
37. This parameter has a two clock minimum requirement at any ^{t}CK.
38. The ^{t}FAW (MIN) parameter applies to all 8-bank DDR2 devices. No more than four bank-ACTIVATE commands may be issued in a given ^{t}FAW (MIN) period. ^{t}RRD (MIN) restriction still applies.
39. The minimum internal READ-to-PRECHARGE time. This is the time from which the last 4-bit prefetch begins to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when ^{t}RTP/(2 × ^{t}CK) > 1, such as frequencies faster than 533 MHz when ^{t}RTP = 7.5ns. If ^{t}RTP/(2 × ^{t}CK) ≤ 1, then equation AL + BL/2 applies. ^{t}RAS (MIN) has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
40. ^{t}DAL = (*n*WR) + (^{t}RP/^{t}CK). Each of these terms, if not already an integer, should be rounded up to the next integer. ^{t}CK refers to the application clock period; *n*WR refers to the ^{t}WR parameter stored in the MR9–MR11. For example, -37E at ^{t}CK = 3.75ns with ^{t}WR programmed to four clocks would have ^{t}DAL = 4 + (15ns/3.75ns) clocks = 4 + (4) clocks = 8 clocks.
41. The refresh period is 64ms (commercial) or 32ms (industrial and automotive) or 8ms(automotive ultra-high temperature). This equates to an average refresh rate of 7.8125µs (commercial) or 3.9607µs (industrial and automotive) or 0.975µs (automotive ultra-high temperature). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms (commercial) or 32ms (industrial and automotive) or 8ms(automotive ultra-high temperature). The JEDEC ^{t}RFC MAX of 70,000ns is not required as bursting of AUTO REFRESH commands is allowed.
42. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition (see Reset).
43. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit, as shown in Figure 1.
44. ^{t}CKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 × ^{t}CK + ^{t}IH.
45. The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47, for ^{t}AOF (MIN) and 2.5 + 0.03, or 2.53, for ^{t}AOF (MAX).
46. ODT turn-on time ^{t}AON (MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
47. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in High-Z. Both are measured from ^{t}AOFD.
48. Half-clock output parameters must be derated by the actual $^{t}ERR_{5per}$ and ^{t}JITdty when input clock jitter is present; this will result in each parameter becoming larger. The parameter ^{t}AOF (MIN) is required to be derated by subtracting both $^{t}ERR_{5per}$ (MAX) and ^{t}JITdty (MAX). The parameter ^{t}AOF (MAX) is required to be derated by subtracting both $^{t}ERR_{5per}$ (MIN) and ^{t}JITdty (MIN).
49. The -187E maximum limit is 2 × ^{t}CK + ^{t}AC (MAX) + 1000 but it will likely be 3 x ^{t}CK + ^{t}AC (MAX) + 1000 in the future.
50. Should use 8 ^{t}CK for backward compatibility.
51. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

52. Self-refresh is not available when Tc > 105C.

Revision History

Rev. B – 06/2018

- Added Important Notes and Warnings section for further clarification aligning to industry standards

Rev. A – 09/2015

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.