FXPS71407

DSI3 and PSI5 compatible absolute and relative pressure sensor

Rev. 3.4 — 29 November 2023 Product data sheet



1 General description

FXPS71407 is a DSI3 and PSI5 compatible pressure sensor.

2 Features

- Pressure range options:
  - 40 kPa to 140 kPa absolute pressure range
  - –40 °C to 125 °C operating temperature range
- DSI3 compatible
  - Discovery mode support for physical location identification
  - Command and response mode support for device configuration
  - Periodic data collection mode support for sensor data transfers
  - Background diagnostics mode support during periodic data collection mode
- PSI5 version 2.1 compatible
  - Compatible modes: P10P-500/3L, P10P-500/4H, A10P-228/1L, P10CRC-xxx/xx, and many others
  - Programmable time slots with 1 µs resolution
  - Selectable baud rate: 125 kBd or 189 kBd
  - 10-bit data length for relative pressure
  - Selectable error detection: even parity, or 3-bit CRC
  - Two-wire programming mode
- Pressure transducer and DSP
  - Redundant pressure transducers
  - Capacitance to voltage converter with anti-aliasing filter
  - Sigma delta ADC plus sinc filter
  - Selectable 370 Hz, 2-pole, or 400 Hz, 3-pole and 4-pole 800 Hz, 1000 Hz low-pass filter for absolute pressure
  - 0.16 Hz, 1-pole LPF for P_0 value
  - 10-bit ΔP/P0 output
- Pb-free 16-pin QFN 4 mm x 4 mm x 1.98 mm package

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
FXPS71407T1	HQFN16	HQFN16, plastic, thermal enhanced quad flat package; no leads; 16 terminals; 0.8 mm pitch; 4 mm x 4 mm x 1.98 mm body	SOT1573-2(SC)
FXPS7140P7T1	HQFN16	HQFN16, plastic, thermal enhanced quad flat package; no leads; 16 terminals; 0.8 mm pitch; 4 mm x 4 mm x 1.98 mm body	SOT1573-2(SC)

3.1 Ordering options

Table 2. Ordering options

Basic type[1]	Absolute pressure range	Accuracy[2]	Protocol
FXPS71407[3][4]	40 kPa to 140 kPa	±7.0 % (PREL)	DSI3 or PSI5
FXPS7140P7[4]	40 kPa to 140 kPa	±7.0 % (PREL)	PSI5

[1] To order parts in tape and reel, add the T1 suffix to the part number.
[2] ±7.0 % PREL is guaranteed from –40 °C to 85 °C for life
[3] Default protocol is DSI3. One time programmable to PSI5
[4] Refer to Table 105 for part number to protocol register values.

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4 Block diagram

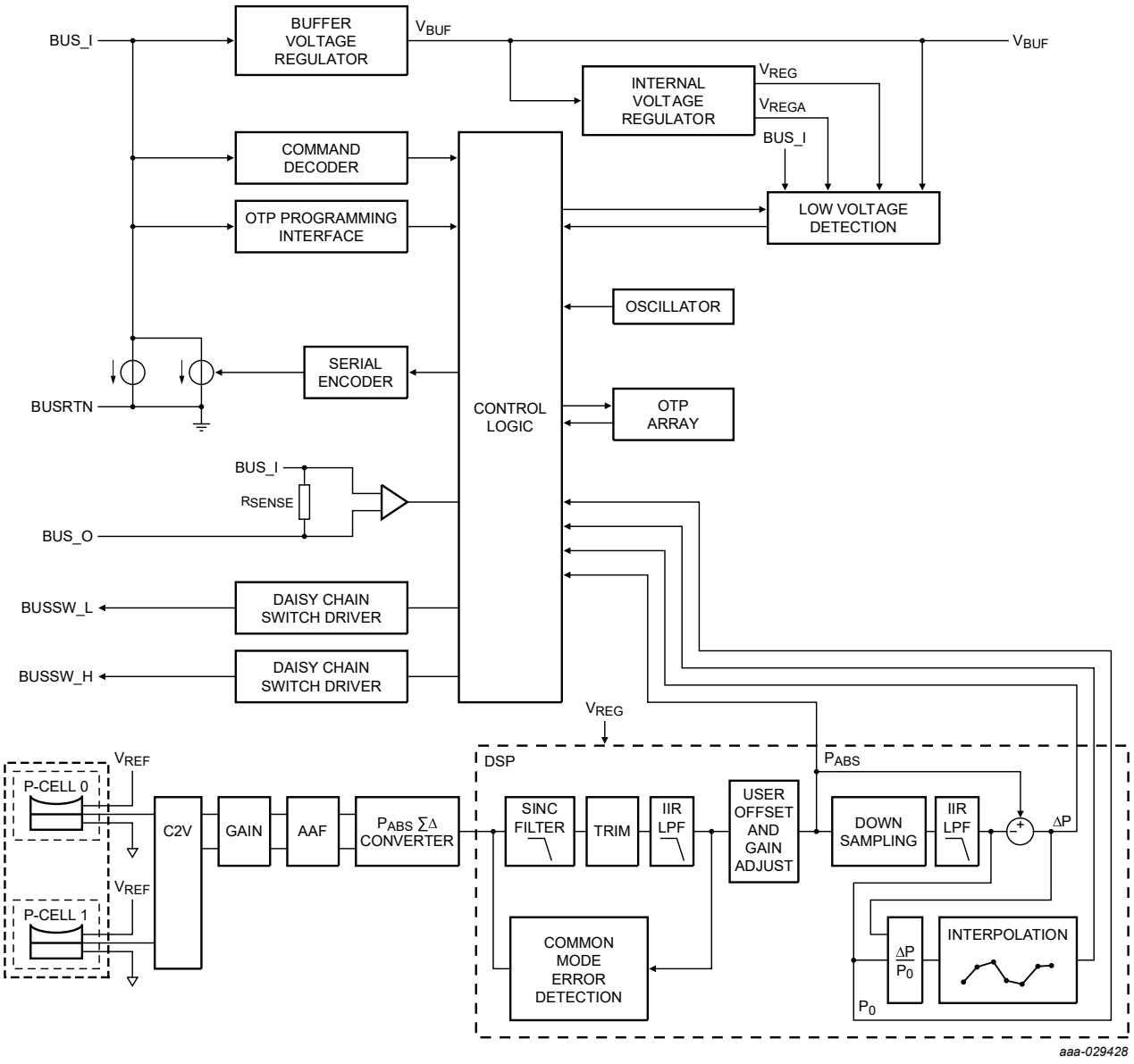


Figure 1. Block diagram

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5 Pinning information

5.1 Pinning

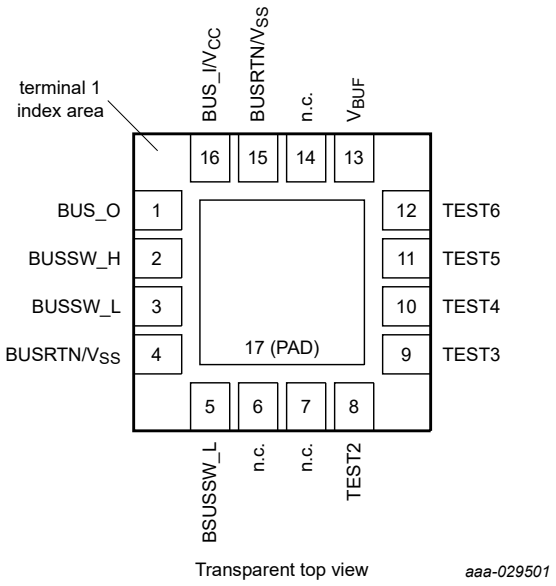


Figure 2. Pin configuration for HQFN16

Table 3. Pin description

Symbol	Pin	Type	Definition
BUS_O	1	Supply out	This pin is connected to the BUS_I pin through an internal sense resistor and provides the supply connection to the next slave in a daisy chain configuration. In DSI3 mode, an external capacitor must be connected between this pin and VSS. In PSI5 mode, NXP recommends that this pin be unterminated. Optionally, this pin can be connected to BUS_I/VCC.
BUSSW_H	2	High-side bus switch driver	In DSI3, switch connected daisy chain mode, this pin is connected to the gate of a P-channel FET which connects BUS_I to the next slave in the daisy chain. An external pullup resistor is required on the gate of the P-channel FET. If unused, or in PSI5 mode, it is recommended that this pin be unterminated. Optionally, this pin can be tied to V_{SS}.
BUSSW_L	3, 5	Low-side bus switch driver	In PSI5 daisy chain mode, this pin is connected to the gate of an N-channel FET which connects BUSRTN to the next slave in the daisy chain. An external pulldown resistor is required on the gate of the N-channel FET as shown in Figure 61. If unused, or in DSI3 mode, NXP recommends that this pin be unterminated. Optionally, this pin can be tied to V_{SS}.
BUSRTN/V_{SS}	4, 15	Supply return	These pins are the supply return nodes.
TEST6	12	Test pin	It is recommended that this pin be unterminated. Optionally, this pin can be tied to V_{SS}.
NC	6, 7, 14	No connect	These pins are not internally connected and can be left unconnected in the application.
TEST2	8	Test pin	In DSI3 or PSI5 mode, it is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{BUF}.
TEST3	9	Test pin	In DSI3 or PSI5 mode, it is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{SS}.
TEST4	10	Test pin	In DSI3 or PSI5 mode, it is recommended that this pin be unterminated. Optionally, this pin can be connected to V_{SS}.
TEST5	11	Test pin	In DSI3 or PSI5 mode, this pin must be left unconnected.
V_{BUF}	13	Power supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies the internal regulators to provide immunity from EMC, and supply dropouts. An external capacitor must be connected between this pin and V_{SS} as shown in Figure 59 and Figure 61.
BUS_I/V_{CC}	16	Supply and communication	This pin is connected to the supply line and supplies power to the device. An external capacitor must be connected between this pin and BUSRTN as shown in Section 11 "Application information". This pin also modulates the response current for PSI5 communication and provides the supply for OTP programming. ***Note:*** *BUS_I and VCC are the same.*
PAD	17	Die attach pad	This pin is the die attach flag, and must be connected to V_{SS}. See Section 12.1 "Footprint" for die attach pad connection details.

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6 Functional description

6.1 User accessible data array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification.

Table 4. User accessible data array

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
General device information										
$00	COUNT	R	COUNT[7:0]							
$01	DEVSTAT	R	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
$02	DEVSTAT1	R	VBUFUV_ERR	BUSINUV_ERR	VBUFOV_ERR	Reserved	INTREGA_ERR	INTREG_ERR	INTREGF_ERR	CONT_ERR
$03	DEVSTAT2	R	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_W_ACTIVE	Reserved	TEMP0_ERR	Reserved	Reserved
$04	DEVSTAT3	R	Reserved	OSCTRAIN_ERR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$05	COMMREV	R	0	0	0	0	COMMREV[3:0]			
$06 to $0D	Reserved	R	Reserved							
$0E	TEMPERATURE	R	TEMP[7:0]							
$0F	Reserved	R	Reserved							
Communication										
$10	DEVLOCK_WR	R/W	ENDINIT	Reserved	Reserved	Reserved	SUP_ERR_DIS	Reserved	RESET[1:0]	
$11	WRITE_OTP_EN	R/W	UOTP_WR_INIT	Reserved	Reserved	Reserved	EX_COMMTYPE	EX_PADDR	UOTP_REGION[1:0]	
$12	BUSSW_CTRL	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUSSW_CTRL[1:0]	
$13	PSI5_TEST	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PSI5_TEST
$14	UF_REGION_W	R/W	REGION_LOAD[3:0]				0	0	0	0
$15	UF_REGION_R	R	REGION_ACTIVE[3:0]				0	0	0	0
$16	COMMTYPE	UF2	Reserved	Reserved	Reserved	Reserved	Reserved	COMMTYPE[2:0]		
$17	Reserved	UF2	Reserved							
$18	PHYSADDR	UF2	0	0	0	0	PADDR[3:0]			
$19	Reserved	UF2	Reserved							
$1A	SOURCEID_0	UF2	SID0_EN	PDCMFORMAT[2:0]			SOURCEID_0[3:0]			
$1B	SOURCEID_1	UF2	SID1_EN	Reserved	Reserved	Reserved	SOURCEID_1[3:0]			
$1C to $21	Reserved	UF2	Reserved							
$22	TIMING_CFG	UF2	PDCM_PER[2:0]			OSCTRAIN_SEL	CK_CAL_RST	CRM_PER[1:0]		CK_CAL_EN
$23	CHIPTIME	UF2	Reserved	Reserved	Reserved	SS_EN	CHIPTIME[3:0]			
$24	BDM_CFG	UF2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BDM_FRAGSIZE	BDM_EN
$25	PSI5_CFG	UF2	SYNC_PD	DAISY_CHAIN	PSI5_ILOW	DATA_EXT	EMSG_EXT	P_CRC	INIT2_EXT	ASYNC
$26	PDCM_RSPST0_L	UF2	PDM_RSPST0[7:0]							
$27	PDCM_RSPST0_H	UF2	BRC_RSP0[1:0]		Reserved	PDCM_RSPST0[12:8]				
$28	PDCM_RSPST1_L	UF2	PDM_RSPST1[7:0]							
$29	PDCM_RSPST1_H	UF2	BRC_RSP1[1:0]		Reserved	PDCM_RSPST1[12:8]				
$2A-$37	Reserved	UF2	Reserved							
$38	PDCM_CMD_B_L	UF2	PDCM_CMD_B[7:0]							
$39	PDCM_CMD_B_H	UF2	Reserved	Reserved	Reserved	PDCM_CMD_B[12:8]				
$3A-$3F	Reserved	UF2	Reserved							

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Table 4. User accessible data array *...continued*

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
Sensor specific information										
$40	DSP_CFG_U1	UF2	LPF[3:0]				Reserved			
$41	DSP_CFG_U2	UF2	Reserved							
$42	DSP_CFG_U3	UF2	Reserved	DATATYPE0[1:0]		Reserved	DATATYPE1[1:0]		Reserved	Reserved
$43	DSP_CFG_U4	UF2	P0_RESET	Reserved	Reserved	P0_RLD	Reserved	Reserved	Reserved	Reserved
$44	DSP_CFG_U5	UF2	ST_CTRL[3:0]				Reserved	Reserved	Reserved	Reserved
$45	Reserved	UF2	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved
$46	P_INT_HI_L	UF2	P_INT_HI[7:0]							
$47	P_INT_HI_H	UF2	P_INT_HI[15:8]							
$48	P_INT_LO_L	UF2	P_INT_LO[7:0]							
$49	P_INT_LO_H	UF2	P_INT_LO[15:8]							
$4A	Reserved	UF2	Reserved							
$4B	Reserved	UF2	Reserved							
$4C	P_CAL_ZERO_L	UF2	P_CAL_ZERO[7:0]							
$4D	P_CAL_ZERO_H	UF2	P_CAL_ZERO[15:8]							
$4E	Reserved	UF2	Reserved							
$4F to $5E	Reserved	UF2	Reserved							
$5F	CRC_UF2	F	LOCK_UF2	0	0	0	CRC_UF2[3:0]			
$60	DSP_STAT	R	Reserved	PABS_HIGH	PABS_LOW	Reserved	ST_INCMPLT	ST_ACTIVE	CM_ERROR	ST_ERROR
$61	DEVSTAT_COPY	R	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
$62	SNSDATA0_L	R	SNSDATA0_L[7:0]							
$63	SNSDATA0_H	R	SNSDATA0_H[15:8]							
$64	SNSDATA1_L[7:0]	R	SNSDATA1_L[7:0]							
$65	SNSDATA1_L[15:8]	R	SNSDATA1_L[15:8]							
$66	SNSDATA0_TIME0	R	SNSDATA0_TIME[7:0]							
$67	SNSDATA0_TIME1	R	SNSDATA0_TIME[15:8]							
$68	SNSDATA0_TIME2	R	SNSDATA0_TIME[23:16]							
$69	SNSDATA0_TIME3	R	SNSDATA0_TIME[31:24]							
$6A	SNSDATA0_TIME4	R	SNSDATA0_TIME[39:32]							
$6B	SNSDATA0_TIME5	R	SNSDATA0_TIME[47:40]							
$6C	P_MAX_L	R	P_MAX[7:0]							
$6D	P_MAX_H	R	P_MAX[15:7]							
$6E	P_MIN_L	R	P_MIN[7:0]							
$6F	P_MIN_H	R	P_MIN[15:7]							
$70 to $77	Reserved	R	Reserved							
$78	FRT0	R	FRT[7:0]							
$79	FRT1	R	FRT[15:8]							
$7A	FRT2	R	FRT[23:16]							
$7B	FRT3	R	FRT[31:24]							
$7C	FRT4	R	FRT[39:32]							
$7D	FRT5	R	FRT[47:40]							
$7E to $9F	Reserved	R	Reserved							
$A0 to $AE	Reserved	F	Reserved				Reserved	Reserved	Reserved	Reserved
$AF	CRC_F_A	F	LOCK_F_A	REGA_BLOCKID[2:0]			CRC_F_A[3:0]			
$B0 to $BE	Reserved	F	Reserved							

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Table 4. User accessible data array *...continued*

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
$BF	CRC_F_B	F	LOCK_F_B	REGB_BLOCKID[2:0]			CRC_F_B[3:0]			
Traceability information										
$C0	ICTYPEID	F	ICTYPEID[7:0]							
$C1	ICREVID	F	ICREVID[7:0]							
$C2	ICMFGID	F	ICMFGID[7:0]							
$C3	Reserved	F	Reserved							
$C4	PN0	F	PN0[7:0]							
$C5	PN1	F	PN1[7:0]							
$C6	SN0	F	SN[7:0]							
$C7	SN1	F	SN[15:8]							
$C8	SN2	F	SN[23:16]							
$C9	SN3	F	SN[31:24]							
$CA	SN4	F	SN[39:32]							
$CB	ASICWFR#	F	ASICWFR#[7:0]							
$CC	ASICWFR_X	F	ASICWFR_X[7:0]							
$CD	ASICWFR_Y	F	ASICWFR_Y[7:0]							
$CE	Reserved	F	Reserved							
$CF	CRC_F_C	F	LOCK_F_C	REGC_BLOCKID[2:0]			CRC_F_C[3:0]			
$D0	ASICWLOT_L	F	ASICWLOT_L[7:0]							
$D1	ASICWLOT_H	F	ASICWLOT_H[7:0]							
$D2 to $D9	Reserved	F	Reserved							
$DA to $DE	Reserved	F	Reserved							
$DF	CRC_F_D	F	LOCK_F_D	REGD_BLOCKID[2:0]			CRC_F_D[3:0]			
$E0	USERDATA_0	UF0	USERDATA_0[7:0]							
$E1	USERDATA_1	UF0	USERDATA_1[7:0]							
$E2	USERDATA_2	UF0	USERDATA_2[7:0]							
$E3	USERDATA_3	UF0	USERDATA_3[7:0]							
$E4	USERDATA_4	UF0	USERDATA_4[7:0]							
$E5	USERDATA_5	UF0	USERDATA_5[7:0]							
$E6	USERDATA_6	UF0	USERDATA_6[7:0]							
$E7	USERDATA_7	UF0	USERDATA_7[7:0]							
$E8	USERDATA_8	UF0	USERDATA_8[7:0]							
$E9	USERDATA_9	UF0	USERDATA_9[7:0]							
$EA	USERDATA_A	UF0	USERDATA_A[7:0]							
$EB	USERDATA_B	UF0	USERDATA_B[7:0]							
$EC	USERDATA_C	UF0	USERDATA_C[7:0]							
$ED	USERDATA_D	UF0	USERDATA_D[7:0]							
$EE	USERDATA_E	UF0	USERDATA_E[7:0]							
$EF	CRC_UF0	F	LOCK_UF0	REGE_BLOCKID[2:0]			CRC_UF0[3:0]			
$F0	USERDATA_10	UF1	USERDATA_10[7:0]							
$F1	USERDATA_11	UF1	USERDATA_11[7:0]							
$F2	USERDATA_12	UF1	USERDATA_12[7:0]							
$F3	USERDATA_13	UF1	USERDATA_13[7:0]							
$F4	USERDATA_14	UF1	USERDATA_14[7:0]							
$F5	USERDATA_15	UF1	USERDATA_15[7:0]							
$F6	USERDATA_16	UF1	USERDATA_16[7:0]							
$F7	USERDATA_17	UF1	USERDATA_17[7:0]							
$F8	USERDATA_18	UF1	USERDATA_18[7:0]							
$F9	USERDATA_19	UF1	USERDATA_19[7:0]							
$FA	USERDATA_1A	UF1	USERDATA_1A[7:0]							

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Table 4. User accessible data array*...continued*

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
$FB	USERDATA_1B	UF1	USERDATA_1B[7:0]							
$FC	USERDATA_1C	UF1	USERDATA_1C[7:0]							
$FD	USERDATA_1D	UF1	USERDATA_1D[7:0]							
$FE	USERDATA_1E	UF1	USERDATA_1E[7:0]							
$FF	CRC_UF1	F	LOCK_UF1	REGF_BLOCKID[2:0]			CRC_UF1[3:0]			

[1] Memory type codes
R — Readable register with no OTP
F — User readable register with OTP
UF0 — One time user programmable OTP location region 0
UF1 — One time user programmable OTP location region 1
UF2 — One time user programmable OTP location region 2
R/W — User writable register

6.2 Register definitions

6.2.1 COUNT – rolling counter register (address $00)

The count register is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit prescaler divides the primary oscillator frequency by 1000. Thus, the value in the register increases by one count every 100 µs and the counter rolls over every 25.6 ms.

This register is readable in DSI3 mode or PSI5 diagnostic mode.

Table 5. COUNT – rolling count register – (address $00) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

6.2.2 DEVSTATx – device status registers (address $01-$04)

The device status registers are read-only registers which contain device status information.

These registers are readable in DSI3 mode or PSI5 diagnostic mode.

Table 6. DEVSTAT – device status register – (address $01) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
Access	R	R	R	R	R	R	R	R
Reset	1	Reserved	0	0	x	0	1	1

DSP_ERR – DSP error flag

The DSP error flag is set if a DSP-specific error is present in the pressure signal DSP:

DSP_ERR = DSP_STAT[PABS_HIGH] | DSP_STAT[PABS_LOW] | DSP_STAT[ST_INMCPLT] | DSP_STAT[CM_ERROR] | DSP_STAT[ST_ERROR]

COMM_ERR – communication error flag

The communication error flag is set if any bit in DEVSTAT3 is set:

COMM_ERR = OSCTRAIN_ERR

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MEMTEMP_ERR – memory or temperature error flag

The memory error flag is set if any bit in DEVSTAT2 is set:

MEMTEMP_ERR = F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | TEMP0_ERR

SUPPLY_ERR – supply error flag

The supply error flag is set if any bit in DEVSTAT1 is set:

SUPPLY_ERR = VBUFUV_ERR | BUSINUV_ERR | VBUFOV_ERR | INTREG_ERR | INTREGA_ERR | INTREGF_ERR | CONT_ERR

A common timer is used for all error bits in the DEVSTAT1 register. If any bit in DEVSTAT1 is set, the timer is reset to t_{UVOV_RCV}. When no supply errors are present, the timer is decremented until it reaches zero. This error is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 7. SUPPLY_ERR – supply error flag

SUP_ERR_DIS	DSI3 operating modes (COMMTYPE = 0 and 3)	PSI5 operating mode (COMMTYPE = 1 and 5)
0	No response until the supply monitor timer expires. The sensor data field error code is transmitted for one response after the supply monitor timer expires. All supply errors are cleared by a read of the DEVSTAT1 register through any communication interface or on a data transmission that includes the error in the status field if and only if the timer has reached zero.	No transmissions occur if the timer is nonzero. The error is cleared when the timer reaches zero and normal transmissions resume.
1	No transmissions occur if the timer is nonzero. The error is cleared when the timer reaches zero and normal transmissions resume.	

DEVRES – device reset

The device reset bit is set following a device reset. This error is cleared by a read of the DEVSTAT register through any communication interface or on a data transmission that includes the error in the status field.

Table 8. DEVRES – device reset

DEVRES	Error condition
0	Normal operation
1	Device reset occurred

DEVINIT – device initialization

The device initialization bit is set following either a device reset or a change to any of the following bits: CHx_CFG_U1[7:4]. The bit is cleared once sensor data is valid for read through one of the device communication interfaces ($t_{POR_DataValid}$).

Table 9. DEVINIT – device initialization

DEVINIT	Condition
0	Normal operation
1	Device initialization in process

Table 10. DEVSTAT 1– device status register – (address $02) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	VBUFUV_ERR	BUSINUV_ERR	VBUFOV_ERR	RESERVED	INTREGA_ERR	INTREG_ERR	INTREGF_ERR	CONT_ERR
Access	R	R	R	R	R	R	R	R
Reset	X	X	X	X	X	X	X	0

If no error is present, the register contents are cleared when read twice.

VBUFUV_ERR – V_{BUF} undervoltage error

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The V_{BUF} undervoltage error bit is set if the VBUF voltage falls below the voltage specified in Section 9 "Static characteristics". See Section 6.4 "Voltage regulators" for details on the V_{BUF} undervoltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 11. VBUFUV_ERR – V_{BUF} undervoltage error

VBUFUV_ERR	Error condition
0	No error detected
1	VBUF voltage low

BUSINUV_ERR – BUS IN undervoltage error

The BUS IN undervoltage error bit is set if the BUS_IN voltage falls below the voltage specified in Section 9 "Static characteristics". See Section 6.4 "Voltage regulators" for details on the BUS IN undervoltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 12. BUSINUV_ERR – BUS IN undervoltage error

BUSINUV_ERR	Error condition
0	No error detected
1	BUS_IN voltage low

VBUFOV_ERR – V_{BUF} overvoltage error

The V_{BUF} overvoltage error bit is set if the VBUF voltage rises above the voltage specified in Section 9 "Static characteristics". See Section 6.4 "Voltage regulators" for details on the V_{BUF} overvoltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 13. VBUFOV_ERR – V_{BUF} overvoltage error

VBUFUV_ERR	Error condition
0	No error detected
1	VBUF voltage high

INTREGA_ERR – internal analog regulator voltage out of range error

The internal analog regulator voltage out of range error bit is set if the internal analog regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 14. INTREGA_ERR – internal analog regulator voltage out of range error

INTREGA_ERR	Error condition
0	No error detected
1	Internal analog regulator voltage out of range

INTREG_ERR – internal digital regulator voltage out of range error

The internal digital regulator voltage out of range error bit is set if the internal digital regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

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Table 15. INTREG_ERR – internal digital regulator voltage out of range error

INTREG_ERR	Error condition
0	No error detected
1	Internal digital regulator voltage out of range

INTREGF_ERR – internal OTP regulator voltage out of range error

The internal OTP regulator voltage out of range error bit is set if the internal OTP regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 16. INTREGF_ERR – internal OTP regulator voltage out of range error

INTREGF_ERR	Error condition
0	No error detected
1	Internal OTP regulator voltage out of range

CONT_ERR – continuity monitor error

The continuity monitor passes a low current through a connection around the perimeter of the device and monitors the continuity of the connection. The error bit is set if a discontinuity is detected in the connection. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}. This bit is cleared based on the state of the SUP_ERR_DIS bit in the DEVLOCK_WR register as shown in Table 7.

Table 17. CONT_ERR – continuity monitor error

CONT_ERR	Error condition
0	No error detected
1	Error detected in the continuity of the monitor circuit

Table 18. DEVSTAT2 – device status register – (address $03) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_W_ACTIVE	Reserved	TEMP0_ERR	Reserved	Reserved
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	Reserved	0	Reserved	Reserved

F_OTP_ERR – NXP OTP array error

The factory OTP array error bit is set if a fault is detected in the factory OTP array. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 19. F_OTP_ERR – NXP OTP array error

F_OTP_ERR	Error condition
0	No error detected
1	Error detected in the factory OTP array

U_OTP_ERR – user OTP array error

The user OTP array error bit is set if a fault is detected in the user OTP array. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

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Table 20. U_OTP_ERR – user OTP array error

U_OTP_ERR	Error condition
0	No error detected
1	Error detected in the user OTP array

U_RW_ERR – user read/write array error

When ENDINIT is set, an error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code. If a mismatch is detected in the error detection, the U_RW_ERR bit is set. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 21. U_RW_ERR – user read/write array error

U_RW_ERR	Error condition
0	No error detected
1	Error detected in the user read/write array

U_W_ACTIVE – user OTP write in process status bit

The user OTP write in process status bit is set if a user initiated write to OTP is currently in process. The U_W_ACTIVE bit is automatically cleared once the write to OTP is complete.

Table 22. U_W_ACTIVE – user OTP write in process status bit

U_W_ACTIVE	Status condition
0	No OTP write in process
1	OTP write in process

TEMP0_ERR – temperature error

The temperature error bit is set if an over or under temperature condition exists. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 23. TEMP0_ERR – temperature error

TEMP0_ERR	Error condition
0	No error detected
1	Overtemperature or undertemperature error condition detected

Table 24. DEVSTAT3 – device status register – (address $04) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	OSCTRAIN_ERR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Access	R	R	R	R	R	R	R	R
Reset	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

OSCTRAIN_ERR – oscillator training error

The oscillator training error bit is set if an error detected in either the oscillator training settings, or the master communication timing. See Section 6.5.2 "Oscillator training error handling". Once the error condition is corrected, the OSCTRAIN_ERR bit is cleared after a read of the OSCTRAIN_ERR bit through any communication interface, or by a status transmission including the error status through any communication interface.

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Table 25. OSCTRAIN_ERR – oscillator training error

OSCTRAIN_ERR	Error condition
0	No error detected
1	Oscillator training error. See Section 6.5.2 "Oscillator training error handling"

6.2.3 COMMREV – communication protocol revision register (address $05)

The communication protocol revision register is a read-only register which contains the revision for the communication protocol used.

This register is readable in DSI3 mode or PSI5 diagnostic mode.

Table 26. COMMREV – communication protocol revision register – (address $05) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	COMMREV[3:0]			
Access	R	R	R	R	R	R	R	R
Reset (DSI3)	0	0	0	0	0	0	0	1
Reset (PSI5)	0	0	0	0	0	1	1	0

Note: *The response to a register write of the COMMREV register is a valid response with the register contents equal to 00h.*

6.2.4 TEMPERATURE – temperature register ($0E)

The temperature register is a read-only register which provides a temperature value for the IC. The temperature value is specified in Section 9 "Static characteristics"

Note: *The device is only guaranteed to operate within the temperature limits specified in Section 9 "Static characteristics".*

This includes the performance of the temperature register values.

This register is readable in DSI3 mode or PSI5 diagnostic mode.

Table 27. TEMPERATURE – temperature register – (address $0E) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	TEMP[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	X	X	X	X	X	X	X	X

6.2.5 DEVLOCK_WR – lock register writes register (address $10)

The lock register writes register is a user programmed read/write register which contains the ENDINIT bit and reset control bits.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 28. DEVLOCK_WR – lock register writes register – (address $10) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ENDINIT	Reserved	Reserved	Reserved	SUP_ERR_DIS	Reserved	RESET[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ENDINIT – end initialization bit

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The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVLOCK_WR register. Once set, the ENDINIT bit can only be cleared by a device reset.

When ENDINIT is set, the following occurs:

- An error detection is enabled for all user writable registers. The error detection code is continuously calculated on the user writable registers and verified against a previously calculated error detection code.
- The P_0 filter is forced to its final stage.
- Self-test is disabled and inhibited.
- Register writes are inhibited with the exception of the RESET[1:0] bits in the DEVLOCK_WR register.

In DSI3 mode, when the ENDINIT bit is set, the device is forced to PDCM according to the device settings and no longer responds to CRM commands.

In all PSI5 modes, the ENDINIT bit is automatically set when the device exits initialization phase 3.

SUP_ERR_DIS – supply error reporting disable bit

The supply error disable bit allows the user to disable reporting of the supply errors in the DSI3 PDCM fields. See Table 7.

RESET[1:0] – reset control bits

In DSI3 mode or PSI5 mode, a series of three consecutive register write operations to the reset control bits will result in a device reset. To reset the device, the following register write operations must be performed in consecutive commands and in the order shown in Table 29 or the device will not be reset.

Table 29. Register write operations

Register write to DEVLOCK_WR	RES_1	RES_0	Effect
Register Write 1	0	0	No effect
Register Write 2	1	1	No effect
Register Write 3	0	1	Device RESET

6.2.6 WRITE_OTP_EN – write OTP enable register (address $11)

The write OTP enable register is a user programmed read/write register that allows the user to write the contents of the user programmed OTP array mirror registers to the OTP registers. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 30. WRITE_OTP_EN – write OTP enable register – (address $11) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	UOTP_WR_INIT	Reserved	Reserved	Reserved	EX_COMMTYPE	EX_PADDR	UOTP_REGION[1:0]	
Access	R/W	R/W	R/W	v	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Register writes executed by the user to the user programmed OTP array only update the mirror register contents for the OTP array, not the actual OTP registers. To copy the values to the actual OTP registers, a write must be executed to the WRITE_OTP_EN register with the UOTP_WR_INIT bit set. The state of the UOTP_REGION[1:0], the EX_COMMTYPE, and the EX_PADDR bits in the command determine which region of OTP will be written as shown in Table 31.

Table 31. Writes for OTP registers

EX_COMMTYPE	EX_PADDR	UOTP_REGION[1]	UOTP_REGION[0]	OTP write operation	Special conditions
x	x	0	0	Write the current contents of the UF0 registers to OTP	—
x	x	0	1	Write the current contents of the UF1 registers to OTP	—

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Table 31. Writes for OTP registers*...continued*

EX_COMMTYPE	EX_PADDR	UOTP_REGION[1]	UOTP_REGION[0]	OTP write operation	Special conditions
0	0	1	0	Write the current contents of the UF2 registers to OTP, including the COMMTYPE register and the PHYSADDR register	—
0	1	1	0	Write the current contents of the UF2 registers to OTP, including COMMTYPE and excluding PHYSADDR.	PHYSADDR = 00h after OTP write
1	0	1	0	Write the current contents of the UF2 registers to OTP, excluding COMMTYPE and including PHYSADDR.	User must not overwrite COMMTYPE
1	1	1	0	Write the current contents of the UF2 registers to OTP, excluding COMMTYPE and excluding PHYSADDR.	User must not overwrite COMMTYPE PHYSADDR = 00h after OTP write
x	x	1	1	Reserved for future use	—

The UF0 and UF1 user OTP regions as well as the NXP programmed F OTP regions share common mirror registers. For this reason, writes to the OTP for each region must be completed independently according to the procedure below.

Depending upon the operating mode used, the user will need to write the UF2 values to OTP either with or without the PHYSADDR register and the COMMTYPE register being written. If discovery mode or switch connected daisy chain mode will be used, the PHYSADDR register must remain unprogrammed (0000h). If a preprogrammed bus mode will be used, the PHYSADDR register must be programmed to a nonzero value. To support these two user modes, the EX_PADDR bit is used as described in Table 31.

Once a region is written using the OTP Write sequence, the LOCK_Uxxx bit in the appropriate CRC_xxx register is automatically set, locking the array from future writes. Once a region is locked, an error detection is activated to detect changes to the register values. Register values in the UF2 region can be overwritten using register write commands, but no new values can be written to the OTP.

The procedure for writing to the user OTP array UF0 and UF1 regions is:

1. Read the appropriate CRC_UFx register and confirm the LOCK_Uxx bit is not set.
2. Write the desired values to the user array registers for only the region to be written using the procedures in Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)".
   The user must take care to ensure that the proper data is written to each region. If a register write is executed to a new region, the base address will change to the new region. The previous data written to the register block will remain in the shared registers and will be written to OTP if the Write OTP sequence is completed.
3. Execute a write to the WRITE_OTP_EN register with the appropriate bits set for the desired region to program.
   Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit will remain set.
4. Delay $t_{OTP_WRITE_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write has successfully completed by reading back all of the OTP registers using register read commands as defined in Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)".
6. Repeat steps 1 through 4 for all regions to be programmed.

The procedure for writing to the user OTP array UF2 region is:

1. Read the CRC_UF2 register and confirm the LOCK_UF2 bit is not set.
2. Write the desired values to the user array registers.
3. Execute a write to the WRITE_OTP_EN register with region 2 selected and the EX_COMMTYPE and EX_PADDR bit set as desired.
   Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit will remain set.

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4. Delay $t_{OTP_WRITE_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write successfully completed by reading back all of the OTP registers using register read commands.

6.2.7 BUSSW_CTRL – bus switch control register (address $12)

The bus switch control register is a user programmed read/write register which controls the state of the bus switch output driver. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 32. BUSSW_CTRL – bus switch control register – (address $12) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUSSW_CTRL[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

The BUSSW_CTRL bit controls the state of the BUSSW_L and BUSSW_H pins.

Table 33. State of BUSSW_L and BUSSW_H pins

BUSSW_CTRL[1]	BUSSW_CTRL[0]	BUSSW_L pin state	BUSSW_H pin state
0	0	High impedance: An external pullup or pulldown resistor is required if an external switch is connected	High impedance: An external pullup or pulldown resistor is required if an external switch is connected
0	1	High impedance: An external pullup or pulldown resistor is required if an external switch is connected	High impedance: An external pullup or pulldown resistor is required if an external switch is connected
1	0	Active low	Active low
1	1	Active high	High impedance: An external pullup or pulldown resistor is required if an external switch is connected

Note: *In DSI3 and PSI5 DPM modes, the bus switch is activated upon receipt of the register write command. The bus switch activation may impact the current on the bus and cause corruption of the register write response.*

6.2.8 PSI5_TEST – PSI5 test register (address $13)

The PSI5 test register is a user read/write register that contains the PSI5 test control. This register is included in the user read/write array error detection.

This register is readable and writable in DSI3 mode, or PSI5 diagnostic mode.

Table 34. PSI5_TEST – PSI5 test register – (address $13) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PSI5_TEST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

PSI5_TEST – PSI5 test bit

If PSI5 mode is not enabled in the COMMTYPE, the PSI5 test bit enables a single PSI5 command receive and response transmission to allow for the PSI5 transceiver to be tested in other modes.

When the PSI5_TEST bit is set, the device and system proceed through following process.

- The device switches the BUS_I transceiver to PSI5 mode.
- The system must hold the BUS_I node constant for 2 ms minimum to allow the BUS_I command receiver to capture the average voltage.

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- The system must transmit a sync pulse meeting the specifications in Section 9 "Static characteristics".
- The device will transmit a response to the sync pulse with the following configuration:
  - The sync pulse will be pulled down as configured by the SYNC_PD bit in the PSI5_CFG register.
  - The response will start in the time slot selected in the PDCM_RSPST0 register.
  - The response bit time will be as configured in the CHIPTIME register.
  - The response current will be as configured by the PSI5_ILOW bit in the PSI5_CFG register.
  - Two start bits will be transmitted as specified in Section 11.3.3.2 "PSI5 data transmission".
  - 10 bits of data equal to 2AAh will be transmitted.
  - Error checking bits will be transmitted as configured by the P_CRC bit in the PSI5_CFG register.
- Once the transmission is complete, the PSI5_TEST bit is cleared, and the device returns to the communication mode as defined in the COMMTYPE register.

If the bit is set from DSI3 mode, this process occurs once the device has replied to the write message, regardless of whether the reply attempted was successful.

If PSI5 mode is enabled in the COMMTYPE register, this bit has no impact on device operation or performance.

6.2.9 UF_REGION_x – UF region selection registers (address $14, $15)

The UF region load register is a user read/write register that contains the control bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection. The UF region active register is a read-only register that contains the status bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection.

Table 35. UF_REGION_W – UF region selection register – (address $14) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	REGION_LOAD[3:0]				0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	0	0	0	0	0

The UF_REGION_W register is readable and writable in DSI3 mode or PSI5 diagnostic mode. The UF_REGION_R register is readable in DSI3 mode or PSI5 diagnostic mode.

Table 36. UF_REGION_R – UF region selection register – (address $15) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	REGION_ACTIVE[3:0]				0	0	0	0
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	0	0	0	0	0

The user OTP regions UF0, UF1, and F share a block of 16 registers. Before reading the registers via any communication interface, the user must ensure that the desired OTP registers are loaded into the readable registers. To ensure proper reading of the UF0, UF1, and F registers, follow this procedure:

1. Write the desired address range to be read to the REGION_LOAD[3:0] bits in the UF_REGION_W register using one of the communication interfaces available via the COMMTYPE register.

Table 37. Communication interfaces available via the COMMTYPE register

REGION_LOAD[3:0]				OTP register addresses loaded into the readable registers
0	0	0	0	Not applicable
0	0	0	1	Not applicable
0010 through 1001				Reserved
1	0	1	0	Address Range $A0 through $AF
1	0	1	1	Address Range $B0 through $BF
1	1	0	0	Address Range $C0 through $CF
1	1	0	1	Address Range $D0 through $DF

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Table 37. Communication interfaces available via the COMMTYPE register*...continued*

REGION_LOAD[3:0]				OTP register addresses loaded into the readable registers
1	1	1	0	Address Range $E0 through $EF
1	1	1	1	Address Range $F0 through $FF

2. Delay a minimum of t_{SSN_UF01}.

3. Optional: Execute a register read of the UF_REGION_R register and confirm the REGION_ACTIVE[3:0] bits match the values written to the REGION_LOAD[3:0] bits in the UF_REGION_W register.

Table 38. Optional communication interfaces available via the COMMTYPE register

REGION_ACTIVE[3:0]				OTP register addresses loaded into the readable registers
0	0	0	0	Load of OTP registers is in process
0	0	0	1	The contents of the shared registers has been overwritten by the user
0010 through 1001				Not applicable
1	0	1	0	Address range $A0 through $AF
1	0	1	1	Address range $B0 through $BF
1	1	0	0	Address range $C0 through $CF
1	1	0	1	Address range $D0 through $DF
1	1	1	0	Address range $E0 through $EF
1	1	1	1	Address range $F0 through $FF

4. Execute a register read of the desired registers from the UF0, UF1, or F register section. Complete all desired register reads of the selected UF region.

5. Repeat steps 1 through 4 for the next desired UF region to read.

Note:

- *The user must take care to ensure that the desired registers are addressed. For example, if the REGION_LOAD bits are set to Ah and the user executes a read of address $C2, the contents of registers $A2 will be transmitted. No error detection is included other than a read of the REGION_ACTIVE bits.*
- *For COMMTYPE options with multiple protocol options (COMMTYPE = '000 or '001'), no error detection is included other than a read of the REGION_ACTIVE bits. The user must take care to ensure that the REGION_LOAD, bits are not inadvertently changed by an alternative protocol while executing register reads.*

6.2.10 COMMTYPE – communication type register (address $16)

The communication type register is a user programmed read/write register which contains user-specific configuration information for communication type. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 39. COMMTYPE – communication type register – (address $16) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	COMMTYPE[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

The communication type bits, COMMTYPE[2:0], in the DSP_CFG_U4 register select the available protocols for the device as shown in Table 40.

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Table 40. Available protocols

COMMTYPE[2:0]			Communication protocol		Startup internal self-test	Pin 3 function	BUS_I undervoltage detection
			DSI3[1]	PSI5[2]			
0	0	0	X	—	—	Interrupt	—
0	0	1	—	X	X	BUSSW_L	—
0	1	1	X	—	—	BUSSW_L	X
1	0	1	—	X	X	BUSSW_L	X

[1] Refer to Section 11.2 "DSI3 protocol".
[2] Refer to Section 11.3 "PSI5 protocol".

When writing to this register, care must be taken to prevent from inadvertently disabling the desired communication mode. Communication mode register value changes which disable a protocol, including writes to OTP, will not take effect until a device reset to prevent from disabling a necessary communication method. Table 41 describes how communication mode register changes are handled.

Table 41. Communication mode register changes

Original COMMTYPE	New COMMTYPE	Device effect
0 (DSI3)	1 (PSI5)	Protocol change will not occur until a device reset (assuming the OTP is programmed)

Note:

- *In DSI3 mode (COMMTYPE = 0) and PSI5 mode (COMMTYPE = 1), registers accesses by protocol are completed in the order received. Care must be taken to prevent from incorrect addressing of the F, UF0 and UF1 registers.*
- *If the COMMTYPE register is preprogrammed in OTP to a specific communication type, the user must prevent writes to this register when writing the UF2 register to OTP. If a preprogrammed COMMTYPE register is overwritten and then written to OTP, the UF2 CRC verification will fail.*

6.2.11 PHYSADDR – physical address register (address $18)

The physical address register is a user programmed OTP register which contains the physical address of the slave for use in DSI3. This register is included in the read/write array error detection.

If the physical address stored in the OTP array is zero, the address is assigned either during discovery mode or during command and response mode.

If the physical address stored in the OTP array is nonzero, the device ignores discovery mode and uses the programmed physical address for command and response mode. The physical address register value can be changed by a command and response mode register write command. However, if the UF2 region is locked, the value will always be reset to the OTP array value after a reset.

In PSI5 mode, the PHYSADDR register is readable and writable, but has no impact on device operation or performance.

Table 42. PHYSADDR – physical address register – (address $18) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	PADDR[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

6.2.12 SOURCEID_x – source identification registers (address $1A, $1B)

The source identification registers are user programmed read/write registers that contain the source identification information used for DSI3 PDCM, and PSI5 mode. This register is included in the read/write array error detection.

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These registers are readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 43. SOURCEID_0 – source identification register – (address $1A) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SID0_EN	PDCMFORMAT[2:0]			SOURCEID_0[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 44. SOURCEID_1 – source identification register – (address $1B) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SID1_EN	Reserved	Reserved	Reserved	SOURCEID_1[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SIDx_EN – data source enable bits

The SIDx_EN bits enable the data source for the associated source identification.

PDCMFORMAT[2:0] – PDCM format control bits

In DSI3 mode, the PDCM format control bits set the PDCM field sizes as shown in Table 45. See Section 11.2.4.2 "DSI3 periodic data collection mode response transmission" for PDCM response format details.

Table 45. PDCM field sizes

PDCMFORMAT[2:0]			Source ID field size (bits)	Keep alive counter field size (bits)	Status field size (bits)	Data field size (bits)	Total including CRC (bits)
0	0	0	0	2	4	10	24
0	0	1	4	2	4	10	28
0	1	0	0	0	4	12	24
0	1	1	4	0	4	12	28
1	0	0	0	2	0	10	20
1	0	1	0	0	0	16	24
1	1	0	0	0	4	16	28
1	1	1	4	0	4	16	32

In PSI5 mode, the PDCM format control bits set the PSI5 response format as shown in Table 46. See Section 11.3.3.2 "PSI5 data transmission" for PSI5 response format details.

Table 46. PSI5 response format

PDCMFORMAT[2:0]			Data field size (bits)
0	0	0	10
0	0	1	10
0	1	0	10
0	1	1	10
1	0	0	10
1	0	1	10
1	1	0	10
1	1	1	10

SOURCEID_x – source identification

In PSI5 mode, the SOURCEID_x register values control data transmissions as shown Table 47.

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Table 47. SOURCEID_x register values

Source ID	Source ID enable (SIDx_EN)	Asynchronous mode		Synchronous mode		Daisy chain mode	
		Transmission time	Transmission data	Transmission time reference[1]	Transmitted data reference[2]	Transmission time	Transmitted data
SOURCEID_0	0	t_{ASYNC}	SNSDATA0	NA	NA	See Section 11.3.6 "Daisy chain mode"	SNSDATA0
	1			PDCM_RSPST0	SNSDATA0		
SOURCEID_1	0	NA	NA	NA	NA	NA	NA
	1			PDCM_RSPST1	SNSDATA1		

[1] See Section 6.2.17 "PDCM_RSPSTx_x – DSI3 and PSI5 start time registers (address $26 to $29)".
[2] See Section 6.2.21 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)".

6.2.13 TIMING_CFG – communication timing register (address $22)

The communication timing configuration register is a user programmed read/write register which contains user-specific configuration information for protocol timing. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 48. TIMING_CFG – communication timing register – (address $22) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	PDCM_PER[2:0]			OSCTRAIN_SEL	CK_CAL_RST	CRM_PER[1:0]		CK_CAL_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

PDCM_PER[3:0] – periodic data collection mode period

The periodic data collection mode period selection bits set the data collection mode period to be used by the DSI3 or PSI5 master as shown in Table 49. This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the TIMING_CFG register.

Table 49. Data collection mode periods for oscillator training

PDCM_PER[2]	PDCM_PER[1]	PDCM_PER[0]	Periodic data collection mode period
0	0	0	100 µs
0	0	1	125 µs
0	1	0	250 µs
0	1	1	333 µs
1	0	0	500 µs
1	0	1	800 µs
1	1	0	1000 µs
1	1	1	2000 µs

In DSI3 mode, PDCM, and BDM commands are decoded and responded to regardless of the value of this register as long as the general PDCM timing parameters specified in Section 10 "Dynamic characteristics" are met. See Section 6.5.1 "Oscillator training" for details regarding oscillator training.

In PSI5 synchronous mode, sync pulses are decoded and responded to regardless of the value of this register as long as the general timing parameters specified in Section 10 "Dynamic characteristics" are met. See Section 6.5.1 "Oscillator training" for details regarding oscillator training.

In PSI5 asynchronous mode, oscillator training is not applicable.

In PSI5 diagnostic and programming mode, oscillator training is not applicable.

In PSI5 daisy chain command phase, oscillator training is not applicable.

OSCTRAIN_SEL – oscillator training protocol selection bit

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The oscillator training selection bit selects the protocol to use for oscillator training for the COMMTYPE values that enable multiple protocols as shown in Table 50.

Table 50. Protocol to use for oscillator training

COMMTYPE	OSCTRAIN_SEL	Protocol to use for oscillator training
0	0	DSI3
1	0	PSI5
2 to 15	0	Not applicable, no effect
	1	

CK_CAL_RST – clock calibration value reset

The clock calibration reset bit controls the state of the oscillator training when the CK_CAL_EN bit is cleared as described in Table 52. See Section 6.5.1 "Oscillator training" for details regarding oscillator training.

CRM_PER[1:0] – command and response mode period

In PSI5 mode, the CRM_PER[1:0] bits are readable and writable, but have no impact on device operation or performance.

Table 51. Command and response mode period

CRM_PER[1]	CRM_PER[0]	Command and response mode period (multiples of the periodic data collection mode period)
0	0	1
0	1	2
1	0	4
1	1	8

CK_CAL_EN – clock calibration enable

The clock calibration enable bit enables oscillator training over the PSI5 communication interface. See Section 6.5.1 "Oscillator training" for details regarding oscillator training.

Table 52. CK_CAL_EN and CK_CAL_RST oscillator training

CK_CAL_EN	CK_CAL_RST	Oscillator training
0	0	The oscillator value is maintained at the last trained value prior to clearing the CK_CAL_RST bit.
0	1	The oscillator value is reset to the untrained value with a tolerance specified in Section 10 "Dynamic characteristics".
1	x	Oscillator is trained as specified in Section 6.5.1 "Oscillator training".

6.2.14 CHIPTIME – chip time and bit time register (address $23)

The chip time and bit time register is a user programmed read/write register which contains user-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 53. CHIPTIME – chip time and bit time register – (address $23) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	SS_EN	CHIPTIME[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SS_EN – simultaneous sampling enable

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In PSI5 mode, the simultaneous sampling enable bit selects between one of two data latency methods to accommodate synchronized sampling or simultaneous sampling.

Table 54. SS_EN data latency methods

SS_EN	Data latency
0	Synchronous sampling mode (latency relative to time slot)
1	Simultaneous sampling mode (latency relative to sync pulse)

CHIPTIME – chip time

In PSI5 mode, the CHIPTIME bits set the bit time for the PSI5 response data as described in Table 55.

Table 55. Bit time for the PSI5 response data

CHIPTIME[3]	CHIPTIME[2]	CHIPTIME[1]	CHIPTIME[0]	PSI5			DSI3 PDCM		
				Period time	Baud rate	Slew control	Chip time	Chip rate	Slew control
0	0	0	0	5.3 µs	189 kHz	Enabled	1.0 µs	1000 kHz	Disabled
0	0	0	1	5.3 µs	189 kHz	Enabled	2.0 µs	500.0 kHz	Disabled
0	0	1	0	5.3 µs	189 kHz	Enabled	2.5 µs	400.0 kHz	Enabled
0	0	1	1	5.3 µs	189 kHz	Enabled	2.6 µs	384.6 kHz	Enabled
0	1	0	0	5.3 µs	189 kHz	Enabled	2.6 µs	384.6 kHz	Enabled
0	1	0	1	5.3 µs	189 kHz	Enabled	2.7 µs	370.3 kHz	Enabled
0	1	1	0	5.3 µs	189 kHz	Enabled	2.8 µs	357.1 kHz	Enabled
0	1	1	1	5.3 µs	189 kHz	Enabled	2.9 µs	344.8 kHz	Enabled
1	0	0	0	8.0 µs	125 kHz	Enabled	3.0 µs	333.3 kHz	Enabled
1	0	0	1	8.0 µs	125 kHz	Enabled	3.1 µs	322.6 kHz	Enabled
1	0	1	0	8.0 µs	125 kHz	Enabled	3.2 µs	312.5 kHz	Enabled
1	0	1	1	8.0 µs	125 kHz	Enabled	3.3 µs	303.0 kHz	Enabled
1	1	0	0	8.0 µs	125 kHz	Enabled	3.5 µs	294.1 kHz	Enabled
1	1	0	1	8.0 µs	125 kHz	Enabled	4.0 µs	250.0 kHz	Enabled
1	1	1	0	8.0 µs	125 kHz	Enabled	4.5 µs	222.2 kHz	Enabled
1	1	1	1	8.0 µs	125 kHz	Enabled	5.0 µs	200.0 kHz	Enabled

6.2.15 BDM_CFG – DSI3 background diagnostic mode configuration register (address $24)

The DSI3 background diagnostic mode configuration register is a user programmed read/write register which contains user-specific configuration information for DSI3 background diagnostic mode. This register is included in the read/write array error detection. See Section 11.2.4 "DSI3 periodic data collection mode and background diagnostic mode" for details regarding background diagnostic mode.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 56. BDM_CFG – DSI3 background diagnostic mode configuration register – (address $24) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BDM_FRAGSIZE	BDM_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BDM_FRAGSIZE – background diagnostic mode fragment size

The background diagnostic mode fragment size bit sets the number of background diagnostic command bits and response chips to be sent per periodic data collection mode sampling period.

Table 57. Background diagnostic command bits and response chips

BDM_FRAGSIZE	BDM command fragment size (bits)	BDM response fragment size (chips)
0	2	3

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Table 57. Background diagnostic command bits and response chips...*continued*

BDM_FRAGSIZE	BDM command fragment size (bits)	BDM response fragment size (chips)
1	4	6

In PSI5 mode, the BDM_FRAGSIZE bit is readable and writable, but has no impact on device operation or performance.

BDM_EN – background diagnostic mode enable

The background diagnostic mode enable bit enables background diagnostic mode as described in Table 58. See Section 11.2.4 "DSI3 periodic data collection mode and background diagnostic mode" for details regarding background diagnostic mode.

Table 58. Background diagnostic mode enabled

BDM_EN	Background diagnostic mode
0	Disabled
1	Enabled

In PSI5 mode, the BDM_EN bit is readable and writable, but has no impact on device operation or performance.

6.2.16 PSI5_CFG – PSI5 configuration register (address $25)

The PSI5 configuration register is a user programmable OTP register that contains PSI5 specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 59. PSI5_CFG – PSI5 configuration register – (address $25) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SYNC_PD	DAISY_CHAIN	PSI5_ILOW	DATA_EXT	EMSG_EXT	P_CRC	INIT2_EXT	ASYNC
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SYNC_PD – sync pulse pulldown enable bit

In PSI5 mode, the sync pulse pulldown enable bit selects if the sync pulse pulldown is enabled once a sync pulse is detected. See Section 6.2.17 for more information regarding the sync pulse pulldown.

Table 60. Sync pulse pulldown enable bit select

SYNC_PD	Sync pulse pulldown
0	Disabled
1	Enabled for all PSI5 operating modes

DAISY_CHAIN – PSI5 daisy chain selection bit

In PSI5 mode, the transmission mode selection bits select the PSI5 transmission mode as shown in Table 61.

Table 61. Transmission mode selection bits select

DAISY_CHAIN	Operating mode	Response (PDCM_RSTST0)	Reference
0	Normal mode (asynchronous or parallel, synchronous)	SNSDATA0	Section 11.3.5 "Normal mode"
1	Daisy chain mode	SNSDATA0	Section 11.3.6 "Daisy chain mode"

PSI5 low response current selection bit (PSI5_ILOW)

In PSI5 mode, the PSI5 low response current selection bit selects the low PSI5 response current specified in Section 9 "Static characteristics" as shown in Table 62.

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Table 62. PSI5 low response current

PSI5_ILOW	PSI5 response current
0	Normal response current
1	Low response current

DATA_EXT – data range extension bit

In PSI5 mode, the data range extension bit enables or disables extending the clipping limits for the relative pressure PSI5 data range as shown in Table 63.

Table 63. PSI5 relative pressure PSI5 data range

DATA_EXT	Description
0	Relative pressure data transmitted from –102 to +307 LSB as specified in Section 9 "Static characteristics"
1	Relative pressure data transmitted from –480 to +480 LSB as specified in Section 9 "Static characteristics"

EMSG_EXT – error message information extension bit

In PSI5 mode, the error message information extension bit enables or disables additional PSI5 error message information as shown in Table 64.

Table 64. PSI5 error message information

EMSG_EXT	Description
0	All internal errors map to 1F4h, see Section 11.3.3.4 "PSI5 data field and data range values"
1	Additional PSI5 reserved codes are used for internal error distinction, see Section 11.3.3.4 "PSI5 data field and data range values"

P_CRC – PSI5 response message error detection selection bit

In PSI5 mode, the response message error detection selection bit selects either even parity, or a 3-bit CRC for error detection of the PSI5 response message. See Section 6.2.17 "PDCM_RSPSTx_x – DSI3 and PSI5 start time registers (address $26 to $29)" for details regarding response message error detection.

Table 65. PSI5 response message error detection

P_CRC	Parity or CRC
0	Parity
1	CRC

In DSI3 mode, the P_CRC bit is readable and writable, but has no impact on device operation or performance.

INIT2_EXT – initialization phase 2 data extension bit

In PSI5 mode, the initialization phase 2 data extension bit enables or disables data transmission in data fields D33 through D48 of PSI5 initialization phase 2 as shown in Table 66.

Table 66. D33 through D48 of PSI5 initialization phase 2

INIT2_EXT	Description
0	D33 through D48 are not transmitted
1	D33 through D48 are transmitted as defined in Section 11.3.4.2.1 "PSI5 initialization phase 2 data transmissions"

In DSI3 mode, the INIT2_EXT bit is readable and writable, but has no impact on device operation or performance.

ASYNC – asynchronous mode bit

In PSI5 mode, the asynchronous mode bit enables asynchronous data transmission as described in Section 6.2.17 only if the DAISY_CHAIN bit is not set.

In DSI3 mode, the ASYNC bit is readable and writable, but has no impact on device operation or performance.

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6.2.17 PDCM_RSPSTx_x – DSI3 and PSI5 start time registers (address $26 to $29)

The DSI3 and PSI5 start time registers are user programmed read/write registers which contain user-specific configuration information for DSI3 periodic data collection mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 67. PDCM_RSPSTx_x – DSI3 and PSI5 start time registers – (address $26 to $29) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$26	PDCM_RSPST0_L	PDCM_RSPST0[7:0]							
$27	PDCM_RSPST0_H	BRC_RSP0[1:0]		Reserved	PDCM_RSPST0[12:8]				
$28	PDCM_RSPST1_L	PDCM_RSPST1[7:0]							
$29	PDCM_RSPST0_H	BRC_RSP1[1:0]		Reserved	PDCM_RSPST1[12:8]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

PDCM_RSPSTx[12:0] – periodic data collection mode response start time

The DSI3 periodic data collection mode response start time registers set the periodic data collection mode response start time for the associated data and SOURCEID. The value is stored in 1.0 µs increments.

Table 68. Periodic data collection mode response start time for the associated data and SOURCEID

PDCM_RSPSTx[12:0]	Periodic data collection mode response start time
0	See Table 69.
0 < PDCM_RSPSTx[12:0] < 20	20.0 µs
20 < PDCM_RSPSTx[12:0]	PDCM response start = PDCM_RSPST x 1.0 µs

Table 69 shows the relationship of the SOURCEID, the transmitted data, the response start times, and the default states for each set of registers. Care must be taken to prevent from programming response start times which cause data contention in the system.

Table 69. Default states for SOURCEID_x, SNSDATAxm, PCDM_REPSTx

SOURCEID register	Transmitted data	Start time registers	Default start (PDCM_RSPSTx[12:0] = 00h)
SOURCEID_0	SNSDATA0	PDCM_RSPST0[12:0]	Transmit data with a start time of 20 µs
SOURCEID_1	SNSDATA1	PDCM_RSPST1[12:0]	Transmit data with a start time of 20 µs

Table 70 shows the PSI5 data transmission start times based on the values in the PDCM_RSPSTx registers and the value of the ASYNC bit. Care must be taken to prevent from programming time slots which violate the PSI5 Version 1.3 specification, or time slots which will cause data contention.

Table 70. PSI5 data transmission start times

ASYNC Bit	SOURCEID register	Transmitted data	Time slot start time	Default start (PDCM_RSPSTx[12:0] = 00h)
1	SOURCEID_0	SNSDATA0	Asynchronous mode	t_{ASYNC}
0	SOURCEID_0	SNSDATA0	PDCM_RSPST0[12:0]	Transmit data with a start time of 20 µs.
	SOURCEID_1	SNSDATA1	PDCM_RSPST1[12:0]	Transmit data with a start time of 20 µs.

BRC_RSP[1:0] – broadcast read command type selection bits

The broadcast read command type selection bits select the broadcast read command types that the device responds to for each source ID as shown in Table 71.

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Table 71. BRC_RSP[1:0] response

BRC_RSP[1]	BRC_RSP[0]	Response
0	0	Respond to all broadcast read commands
0	1	Respond to broadcast read command 0 only
1	0	Respond to broadcast read command 1 only
1	1	Respond to all broadcast read commands

If a device is programmed to respond only to BRC0 or BRC1 commands, it will synchronize to alternate responses when BDM commands are received.

- If the last command prior to a BDM command is a BRC0, a device programmed to respond only to BRC0 commands will not respond to the first BDM command and will then respond to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC0, a device programmed to respond only to BRC1 commands will respond to the first BDM command, and will then response to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC1, a device programmed to respond only to BRC0 commands will respond to the first BDM command, and will then response to every other BDM command until the next BRC command is received.
- If the last command prior to a BDM command is a BRC1, a device programmed to respond only to BRC1 commands will not respond to the first BDM command and will then respond to every other BDM command until the next BRC command is received.

In PSI5 mode, the BRC_RSP[1:0] bits are readable and writable, but have no impact on device operation or performance.

6.2.18 PDCM_CMD_B_x – DSI3 and PSI5 command blocking time registers (address $38, $39)

The DSI3 and PSI5 command blocking registers are user programmed read/write registers which contain user-specific configuration information for DSI3 mode and PSI5 mode. These registers are included in the read/write array error detection.

These registers are readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 72. PDCM_CMD_B_x – DSI3 and PSI55 command blocking time registers – (address $38, $39) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$38	PDCM_CMD_B_L	PDCM_CMD_B[7:0]							
#39	PDCM_CMD_B_H	Reserved	Reserved	Reserved	PDCM_CMD_B[12:8]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

In DSI3 mode, the DSI3 periodic data collection mode command blocking time bits set the periodic data collection mode command blocking time in 1.0 µs increments, with zero as the default value of 450 µs. For proper communication, the command blocking time must exceed the completion of the last source response transmission. See Section 11.2.1.1 "Command receiver" for details regarding the command receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper command decoding in the system and to ensure proper sampling of the VHIGH voltage. As shown in Section 11.2.1.1 "Command receiver", the VHIGH voltage is initially captured at the end of the command blocking time and then filtered. The user must ensure that the command blocking end time is set for a time when no command or response transmissions are occurring to provide the most stable BUS_I voltage.

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Table 73. DSI3 mode sync pulse blocking time

PDCM_CMD_B[12:0]	Sync pulse blocking time
0	450 µs
Nonzero	Sync pulse blocking time = PDCM_CMD_B x 1 µs

In PSI5 mode, the command blocking time bits set the PSI5 sync pulse blocking time in 1.0 µs increments, with zero as the default value of 450 µs. See Section 11.3.2.1 "Synchronization pulse" for details regarding the PSI5 sync pulse receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper sync pulse decoding in the system and to ensure proper sampling of the PSI5 voltage.

Table 74. PSI5 mode sync pulse blocking time

PDCM_CMD_B[12:0]	Sync pulse blocking time
0, 1, 2, 3, 4, 5, 6, 7, 8, 9	450 µs
10 to 8191	Sync pulse blocking time = PDCM_CMD_B x 1 µs

6.2.19 WHO_AM_I – who am I register (address $3E)

The Who_Am_I register is a user programmed read/write register which contains the unique product identifier. The register is readable in all modes. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 75. WHO_AM_I – who am I register – (address $3E) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WHO_AM_I[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Factory default stored value	0	0	0	0	0	0	0	0
Factory default read value	1	1	0	0	0	1	0	0

The default register value is 00h. If the register value is 00h, a value of C4h is transmitted in response to a read command. For all other register values, the actual register value is transmitted in response to a read command.

Table 76. Response to a register read command

WHO_AM_I register value (hex)	Response to a register read command
00h	C4h
01h Through FFh	Actual register value

6.2.20 DSP_CFG_U1 – DSP user configuration #1 register (address $40)

The DSP user configuration register #1 is a user programmable read/write register which contains DSP-specific configuration information. This register is included in the read/write array error detection.

Changes to this register reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 10 "Dynamic characteristics". Reads of the SNSDATA_x registers and sensor data requests should be prevented during this time.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 77. DSP_CFG_U1 – DSP user configuration #1 register – (address $40) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	LPF[3:0]				Reserved	Reserved	Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 77. DSP_CFG_U1 – DSP user configuration #1 register – (address $40) bit allocation...*continued*

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0

LPF[3:0] – low-pass filter selection bits

The low-pass filter selection bits select the low-pass filter for the DSP. See Section 6.6.4.3 "Low-pass filter" for details regarding the low-pass filter.

Table 78. LPF[3:0] – low-pass filter selection bits

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low-pass filter type
0	0	0	0	370 Hz, 2-pole
0	0	0	1	400 Hz, 3-pole
0	0	1	0	800 Hz, 4-pole
0	0	1	1	1000 Hz, 4-pole
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	x	x	x	Reserved

6.2.21 DSP_CFG_U3 – DSP user configuration #3 register (address $42)

The DSP user configuration register #3 is a user programmable read/write register which contains DSP-specific configuration information. This register is included in the read/write array error detection.

Changes to this register reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 10 "Dynamic characteristics". Reads of the SNSDATA_x registers and sensor data requests should be prevented during this time.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 79. DSP_CFG_U3 – DSP user configuration #3 register – (address $42) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	DATATYPE0[1:0]		Reserved	DATATYPE1[1:0]		Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

DATATYPE0 – DSP data type 0 selection bits

The DSP data type 0 selection bits select the type of data to be included in the SNSDATA0_L and SNSDATA0_H registers.

Table 80. DSP data type 0 selection bits

DATATYPE0[1]	DATATYPE0[0]	SNSDATA register contents	DSI3 data transmission	PSI5 data transmission
0	0	Relative pressure	Relative pressure	Relative pressure
0	1	Absolute pressure (P_{ABS})	Absolute pressure (P_{ABS})	1F4h
1	0	Filtered absolute pressure (P_0)	Filtered absolute pressure (P_0)	1F4h
1	1	Temperature	Temperature	Temperature

DATATYPE1 – DSP data type 1 selection bits

The DSP data type 1 selection bits select the type of data to be included in the SNSDATA1_L and SNSDATA1_H registers.

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Table 81. DSP data type 1 selection bits

DATATYPE1[1]	DATATYPE1[0]	SNSDATA register contents	DSI3 data transmission	PSI5 data transmission
0	0	Relative pressure	Relative pressure	Relative pressure
0	1	Absolute pressure (P_{ABS})	Absolute pressure (P_{ABS})	1F4h
1	0	Filtered absolute pressure (P_0)	Filtered absolute pressure (P_0)	1F4h
1	1	Temperature	Temperature	Temperature

Note: *Interpolation is not included on the DATATYPE1 output.*

6.2.22 DSP_CFG_U4 – DSP user configuration #4 register (address $43)

The DSP user configuration register #4 is a user programmable read/write register which contains DSP-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 82. DSP_CFG_U4 – DSP user configuration #4 register – (address $43) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	P0_RESET	Reserved	Reserved	P0_RLD	Reserved	INT_OUT	Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

P0_RESET – P_0 filter reset bit

The P_0 filter reset bit provides the option restart P_0 low-pass filter fast startup at phase 0. See Section 6.6.4.4 "P0 low-pass filter and gradient filter" for details regarding the P_0 filter. If a register write to DSP_CFG_U4 occurs with the P0_RESET bit set, 1, and the bit was previously cleared, 0, the P_0 low-pass filter fast startup phase will be reset to phase 0.

Table 83. P_0 filter reset bit

P0_RESET (previous state)	P0_RESET (new state)	P_0 filter startup
0	0	No effect
0	1	Restart the P_0 startup at phase 0
1	0	No effect
1	1	No effect

P0_RLD – P_0 filter rate limiting bypass bit

The P_0 filter rate limiting bypass bit provides the option to bypass the P_0 filter rate limiting after the high-pass filter. See Section 6.6.4.4 "P0 low-pass filter and gradient filter" for details regarding the P_0 filter.

Table 84. P0_RLD – P_0 filter rate limiting bypass bit

P0_RLD	P_0 filter rate limiting
0	Enabled
1	Bypassed

INT_OUT – interrupt pin configuration

The interrupt pin configuration bit selects the mode of operation for the interrupt pin if the pin is enabled. The interrupt output pin is enabled in as shown in Section 6.2.10 "COMMTYPE – communication type register (address $16)". If the pin is enabled, the operating mode is as shown in Table 85. If disabled, the interrupt output pin is high impedance.

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Table 85. INT_OUT – interrupt pin configuration

INT_OUT	Output type
0	Open drain, active high with pulldown current
1	Open drain, active low with pullup current

6.2.23 DSP_CFG_U5 – DSP user configuration #5 register (address $44)

The DSP user configuration register #5 is a user programmable read/write register which contains DSP-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in DSI3 mode or PSI5 diagnostic mode.

Table 86. DSP_CFG_U5 – DSP user configuration #5 register – (address $44) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ST_CTRL[3:0]				Reserved	Reserved	Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ST_CTRL[3:0] – self-test control bits

The self-test control bits select one of the various analog and digital self-test features of the device as shown in Table 87. The self-test control bits are not included in the read/write array error detection.

Table 87. Self-test control bits

ST_CTRL[3]	ST_CTRL[2]	ST_CTRL[1]	ST_CTRL[0]	Function	SNS_DATAx_X contents
					16-bit data
0	0	0	0	Normal pressure signal	Sensor data as specified in Section 6.2.21 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)"
0	0	0	1	P-Cell common mode verification	Sensor data as specified in Section 6.2.21 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)"
0	0	1	0	Reserved	Reserved
0	0	1	1	Reserved	Reserved
0	1	0	0	DSP write to SNS_DATAx_X registers inhibited.	0000h
0	1	0	1	DSP write to SNS_DATAx_X registers inhibited.	AAAAh
0	1	1	0	DSP write to SNS_DATAx_X registers inhibited.	5555h
0	1	1	1	DSP write to SNS_DATAx_X registers inhibited.	FFFFh
1	0	0	0	Reserved	Reserved
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Digital self-test 0	See Section 6.6.2.2 "Startup digital self-test verification"
1	1	0	1	Digital self-test 1	See Section 6.6.2.2 "Startup digital self-test verification"
1	1	1	0	Digital self-test 2	See Section 6.6.2.2 "Startup digital self-test verification"
1	1	1	1	Digital self-test 3	See Section 6.6.2.2 "Startup digital self-test verification"

6.2.24 INT_CFG – interrupt configuration register (address $45)

The interrupt configuration register contains configuration information for the interrupt output.

This register can be written during initialization but is locked once the ENDINIT bit is set. Refer to Section 6.2.5 "DEVLOCK_WR – lock register writes register (address $10)". The register is included in the read/write array error detection.

Table 88. INT_CFG – interrupt configuration register – (address $45) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	INT_PS[1:0]		INT_POLARITY	Reserved	Reserved	Reserved

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Table 88. INT_CFG – interrupt configuration register – (address $45) bit allocation...*continued*

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

INT_PS[1:0] – interrupt output pulse stretch

The INT_PS[1:0] bits set the programmable pulse stretch time for the interrupt output. Pulse stretch times are derived from the internal oscillator, so the tolerance on this oscillator applies.

Table 89. Interrupt output pulse stretch

INT_PS[1]	INT_PS[0]	Pulse stretch time (typical oscillator)
0	0	0 ms
0	1	16.000 ms to 16.512 ms
1	0	64.000 ms to 64.512 ms
1	1	256.000 ms to 256.512 ms

If the pulse stretch function is programmed to '00', the interrupt pin is asserted if and only if the interrupt condition exists after the most recent evaluated sample. The interrupt pin is deasserted if and only if an interrupt condition does not exist after the most recent evaluated sample.

If the pulse stretch function is programmed to a nonzero value, the interrupt pin is controlled only by the value of the pulse stretch timer value. If the pulse stretch timer value is nonzero, the interrupt pin is asserted. If the pulse stretch timer is zero, the interrupt pin is deasserted. The pulse stretch counter continuously decrements until it reaches zero. The pulse stretch counter is reset to the programmed pulse stretch value if and only if an interrupt condition exists after the most recent evaluated sample.

INT_POLARITY – interrupt window comparator polarity

The interrupt polarity bit controls whether the interrupt is activated for values within or outside the window selected by the high and low threshold registers as shown in Table 90. With this bit and the programmable thresholds, a window comparator can be programmed for activation either within or outside a window.

Table 90. Interrupt window comparator polarity

INT_POLARITY	Window comparator type
0	Interrupt activated if the value is outside the window
1	Interrupt activated if the value is inside the window

6.2.25 P_CAL_ZERO_x – pressure calibration registers (address $4C, $4D)

The pressure calibration registers contain user programmable values to adjust the offset of the absolute pressure.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 6.2.5 "DEVLOCK_WR – lock register writes register (address $10)". The register is included in the read/write array error detection. Changes to this register reset the DSP data path. The contents of the SNSDATA_x registers are not guaranteed until the DSP has completed initialization as specified in Section 10 "Dynamic characteristics". Reads of the SNSDATA_x registers and sensor data requests should be prevented during this time.

Table 91. P_CAL_ZERO_x – pressure calibration registers – (address $4C) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$4C	P_CAL_ZERO_L	P_CAL_ZERO[7:0]							
$4D	P_CAL_ZERO_H	P_CAL_ZERO[15:8]							

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Table 91. P_CAL_ZERO_x – pressure calibration registers – (address $4C) bit allocation*...continued*

Address	Name	Bit							
		7	6	5	4	3	2	1	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

The P_CAL_ZERO register value is a signed 16-bit value that is directly added to the internally calibrated pressure signal value as shown in Equation 1. Equation 1 applies to the values in the 16-bit SNSDATA registers. See Section 6.6.4.7 "Output scaling equations" for the default transfer functions for each data output type.

$$PABS_{LSB} = SNSDATA + User \quad Offset \tag{1}$$

Note: *The pressure calibration registers enable range and resolution options beyond the specified values of the device. The user must take care to ensure that the value stored in this register does not result in a compressed output range or a railed output.*

6.2.26 DSP_STAT – DSP-specific status register (address $60)

The DSP status register is a read-only register which contains sensor data-specific status information.

This register is readable in DSI3 mode or PSI5 diagnostic mode.

Table 92. DSP_STAT – DSP-specific status register – (address $60) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	PABS_HIGH	PABS_LOW	Reserved	ST_INCMPLT	ST_ACTIVE	CM_ERROR	ST_ERROR
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	1	0	0	0

PABS_HIGH – absolute pressure out of range high status bit

The absolute pressure out of range high status bit is set if the absolute pressure exceeds the absolute pressure out of range high limit specified in Section 9 "Static characteristics". The PABS_HIGH bit is cleared on a read of the DSP_STAT register through any communication interface or on a data transmission that includes the error in the status field.

PABS_LOW – absolute pressure out of range low status bit

The absolute pressure out of range low status bit is set if the absolute pressure exceeds the absolute pressure out of range low limit specified in Section 9 "Static characteristics". The PABS_LOW bit is cleared on a read of the DSP_STAT register through any communication interface or on a data transmission that includes the error in the status field.

ST_INCMPLT – self-test incomplete

The self-test incomplete bit is set after a device reset and is only cleared when one of the analog or digital self-test modes is enabled in the ST_CTRL register (ST_CTRL[3] = 1 | ST_CTRL[2] = 1 | | ST_CTRL[1] = 1 | | ST_CTRL[0] = 1) or the PSI5 internal self-test procedure has started.

Table 93. Self-test incomplete

ST_INCMPLT	Condition
0	An analog or digital self-test has been activated since the last reset.
1	No analog or digital self-test has not been activated since the last reset AND the PSI5 internal self-test procedure has not completed.

ST_ACTIVE – self-test active flag

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The self-test active bit is set if any self-test mode is currently active, including the PSI5 internal self-test. The self-test active bit is cleared when no self-test mode is active.

ST_ACTIVE = ST_CTRL[3] | ST_CTRL[2] |ST_CTRL[1] | ST_CTRL[0]

CM_ERROR – absolute pressure common mode error status bit

The absolute pressure common mode error status bit is set if the startup common mode self-test value exceeds predetermined limits. The CM_ERROR bit is cleared on a read of the DSP_STAT register through any communication interface or on a data transmission that includes the error in the status field. See Section 6.6.6 "Common mode error detection signal chain" for details regarding the common mode error detection.

ST_ERROR – self-test error flag

The self-test error flag is set if an internal self-test fails as described in Section 6.6.2 "Self-test functions". This bit can only be cleared by a device reset.

6.2.27 DEVSTAT_COPY – device status copy register (address $61)

The device status copy register is a read-only register which contains a copy of the device status information contained in the DEVSTAT register. See Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)" for details regarding the DEVSTAT register contents.

This register is readable in DSI3 mode or PSI5 diagnostic mode. A read of the DEVSTAT_COPY register has the same effect as a read of the DEVSTAT register.

Table 94. DEVSTAT_COPY – device status copy register – (address $61) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
Access	R	R	R	R	R	R	R	R
Reset	Refer to Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)"							

6.2.28 SNSDATA0_L, SNSDATA0_H – sensor data #0 registers (address $62, $63)

The sensor data #0 registers are read-only registers which contain the 16-bit sensor data. The data type for the sensor data #0 registers is selected by the DATATYPE0 bits in the DSP_CFG_U3 register. See Section 6.2.21 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)". See Section 6.6.4.7 "Output scaling equations" for details regarding the 16-bit sensor data.

These registers are readable in DSI3 mode or PSI5 diagnostic mode.

Table 95. SNSDATA0_L, SNSDATA0_H – sensor data #0 registers – (address $62, $63) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$62	SNSDATA0_L	SNSDATA0_L[7:0]							
$63	SNSDATA0_H	SNSDATA0_H[15:8]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.29 SNSDATA1_L, SNSDATA1_H – sensor data #1 registers (address $64, $65)

The sensor data #1 registers are read-only registers which contain the 16-bit sensor data. The data type for the sensor data #1 registers is selected by the DATATYPE0 bits in the DSP_CFG_U3 register. See Section 6.2.21 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)". See Section 6.6.4.7 "Output scaling equations" for details regarding the 16-bit sensor data.

These registers are readable in DSI3 mode or PSI5 diagnostic mode.

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Table 96. SNSDATA0_L, SNSDATA0_H – sensor data #0 registers – (address $62, $63) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$64	SNSDATA1_L	SNSDATA1_L[7:0]							
$65	SNSDATA1_H	SNSDATA1_H[15:8]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.30 SNSDATA0_TIMEx – sensor data 0 timestamp (address $66 to $69, $6A, $6B)

The sensor data 0 timestamp registers are read-only registers which contain a 48-bit timestamp.

These registers are readable in DSI3 mode or PSI5 diagnostic mode.

Table 97. SNSDATA0_TIMEx – sensor data 0 timestamp – (address $66 to $69, $6A, $6B) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$66	SNSDATA0_TIME0	SNSDATA0_TIME[7:0]							
$67	SNSDATA0_TIME1	SNSDATA0_TIME[15:8]							
$68	SNSDATA0_TIME2	SNSDATA0_TIME[23:16]							
$69	SNSDATA0_TIME3	SNSDATA0_TIME[31:24]							
$6A	SNSDATA0_TIME4	SNSDATA0_TIME[39:32]							
$6B	SNSDATA0_TIME5	SNSDATA0_TIME[47:40]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.31 P_MAX, P_MIN – minimum and maximum absolute pressure value registers (address $6C to $6F)

The minimum and maximum absolute pressure value registers are read-only registers which contain a sample by sample continuously updated minimum and maximum 16-bit absolute pressure value. The value is reset to 0000h on a write to a DSP_CFG_Ux register that changes the value of the LPF[3:0], DATATYPE0[1:0], DATATYPE1[1:0], or ST_CTRL[3:0].

These registers are readable in DSI3 mode or PSI5 diagnostic mode.

Table 98. P_MAX_x – maximum absolute pressure value register – (address $6C, $6D) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$6C	P_MAX_L	P_MAX[7:0]							
$6D	P_MAX_H	P_MAX[15:7]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

Table 99. P_MIN_x – maximum absolute pressure value register – (address $6E, $6F) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$6E	P_MIN_L	P_MIN[7:0]							
$6F	P_MIN_H	P_MIN[15:7]							
Access		R	R	R	R	R	R	R	R

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Table 99. P_MIN_x – maximum absolute pressure value register – (address $6E, $6F) bit allocation...*continued*

Address	Name	Bit							
		7	6	5	4	3	2	1	0
Reset		0	0	0	0	0	0	0	0

6.2.32 FRTx – free-running timer registers (address $78, $79, $7A to $7D)

The free-running timer registers are read-only registers which contain a 48-bit free running timer. The free-running timer is clocked by the main oscillator frequency and increments every 100 ns.

These registers are readable in DSI3 mode or PSI5 diagnostic mode.

Table 100. FRTx – free-running timer registers (address $78, $79, $7A to $7D) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$78	FRT0	FRT[7:0]							
$79	FRT1	FRT[15:8]							
$7A	FRT2	FRT[23:16]							
$7B	FRT3	FRT[31:24]							
$7C	FRT4	FRT[39:32]							
$7D	FRT5	FRT[47:40]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.33 ICTYPEID – IC type register (address $C0)

The IC type register is a factory programmable OTP register which contains the IC type as defined in Table 101. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for this register.

Table 101. ICTYPEID – IC type register – (address $C0) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ICTYPEID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	0

6.2.34 ICREVID – IC manufacturer revision register (address $C1)

The IC revision register is a factory programmable OTP register which contains the IC revision. The upper nibble contains the main IC revision. The lower nibble contains the sub IC revision. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for this register.

Table 102. ICREVID – IC manufacturer revision register – (address $C1) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ICREVID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

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6.2.35 ICMFGID – IC manufacturer identification register (address $C2)

The IC manufacturer identification register is a factory programmable OTP register which identifies NXP as the IC manufacturer. This register is included in the factory programmed OTP array error detection.

This register is readable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for this register.

Table 103. ICMFGID – IC manufacturer identification register – (address $C2) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ICMFGID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	0

6.2.36 PNx – part number registers (address $C4, $C5)

The part number registers are factory programmed OTP registers which include the numeric portion of the device part number. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for these registers.

Table 104. PNx – part number registers – (address $C4, $C5) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$C4	PN0	PN0[7:0]							
$C5	PN1	PN1[7:0]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 105. Part number registers protocol

PN1[7:0] value (hex)	PN0[7:0] value (hex)	Protocol
14h	0Dh	DSI3
14h	0Eh	PSI5
14h	0Fh	Generic
Reserved	Reserved	Reserved

6.2.37 SNx – device serial number registers (address $C6 to $C9, $CA)

The serial number registers are factory programmed OTP registers which include the unique serial number of the device. Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 14-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for these registers.

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Table 106. SNx – device serial number registers – (address $C6 to $C9, $CA) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$C6	SN0	SN[7:0]							
$C7	SN1	SN[15:8]							
$C8	SN2	SN[23:16]							
$C9	SN3	SN[31:24]							
$CA	SN4	SN[39:32]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

6.2.38 ASIC wafer ID registers (address $CB to $CD, $D0, $D1)

The ASIC wafer ID registers are factory programmed OTP registers which include the wafer number, and wafer X and Y coordinates for the device ASIC. These registers are included in the factory programmed OTP array error detection.

These registers are readable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for these registers.

Table 107. ASICWFR# – ASIC wafer ID register – (address $CB) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ASICWFR#[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 108. ASICWFR_x – ASIC wafer x, y coordinates ID registers – (address $CC, $CD) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$CC	ASICWFR_X	ASICWFR_X[7:0]							
$CD	ASICWFR_Y	ASICWFR_X[7:0]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 109. ASICWLOT_x – ASIC wafer lot ID registers – (address $D0, $D1) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$D0	ASICWLOT_L	ASICWLOT_L[7:0]							
$D1	ASICWLOT_H	ASICWLOT_H[7:0]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

6.2.39 USERDATA_0 to USERDATA_E – user data registers (address $E0 to $E9, $EA to $EE)

User data registers are user programmable OTP registers which contain user-specific information. These registers are included in the user programmed OTP array error detection.

These registers are readable and writable in DSI3 mode or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for these registers.

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Table 110. USERDATA_X – user data registers (address $E0 to $E9, $EA to $EE) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$E0	USERDATA_0	USERDATA_0[7:0]							
$E1	USERDATA_1	USERDATA_1[7:0]							
$E2	USERDATA_2	USERDATA_2[7:0]							
$E3	USERDATA_3	USERDATA_3[7:0]							
$E4	USERDATA_4	USERDATA_4[7:0]							
$E5	USERDATA_5	USERDATA_5[7:0]							
$E6	USERDATA_6	USERDATA_6[7:0]							
$E7	USERDATA_7	USERDATA_7[7:0]							
$E8	USERDATA_8	USERDATA_8[7:0]							
$E9	USERDATA_9	USERDATA_9[7:0]							
$EA	USERDATA_A	USERDATA_A[7:0]							
$EB	USERDATA_B	USERDATA_B[7:0]							
$CB	USERDATA_C	USERDATA_C[7:0]							
$ED	USERDATA_D	USERDATA_D[7:0]							
$EE	USERDATAEE	USERDATA_E[7:0]							
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

6.2.39.1 PSI5 initialization phase 2 data transmissions of user data

In PSI5 mode, the values of the user data registers are transmitted in initialization phase 2 as shown in Table 111. See Section 11.3.4.2.1 "PSI5 initialization phase 2 data transmissions" for details on the PSI5 initialization phase 2 transmissions.

Table 111. Phase 2 USERDATA_X – user data registers (address $E0 to $E9, $EA to $EE) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$E0	USERDATA_0	Reserved				F1: D1			
$E1	USERDATA_1	F3: D5				F3: D4			
$E2	USERDATA_2	F4: D7				F4: D6			
$E3	USERDATA_3	F5: D9				F5: D8			
$E4	USERDATA_4	F6: D11				F6: D10			
$E5	USERDATA_5	F7: D13				F7: D12			
$E6	USERDATA_6	F9: D32				F7: D14			
$E7	USERDATA_7	F8: D16				F8: D15			
$E8	USERDATA_8	F8: D18				F8: D17			
$E9	USERDATA_9	Reserved				Reserved			
$EA	USERDATA_A	Reserved				Reserved			
$EB	USERDATA_B	Reserved				Reserved			
$EC	USERDATA_C	Reserved				Reserved			
$ED	USERDATA_D	Reserved				Reserved			
$EE	USERDATA_E	Reserved				Reserved			
Access									
Reset		0	0	0	0	0	0	0	0

6.2.40 USERDATA_10 to USERDATA_1E – user data registers (address $F0 to $F9, $FA to $FE)

User data registers are user programmable OTP registers which contain user-specific information. These registers are included in the user programmed OTP array error detection.

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These registers are readable and writable in DSI3 mode, or PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.9 "UF_REGION_x – UF region selection registers (address $14, $15)" for details on the register read process for these registers.

Table 112. USERDATA_10 to USERDATA_1E – user data registers (address $F0 to $F9, $FA to $FE) – bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$F0	USERDATA_10	USERDATA_10[7:0]							
$F1	USERDATA_11	USERDATA_11[7:0]							
$F2	USERDATA_12	USERDATA_12[7:0]							
$F3	USERDATA_13	USERDATA_13[7:0]							
$F4	USERDATA_14	USERDATA_14[7:0]							
$F5	USERDATA_15	USERDATA_15[7:0]							
$F6	USERDATA_16	USERDATA_16[7:0]							
$F7	USERDATA_17	USERDATA_17[7:0]							
$F8	USERDATA_18	USERDATA_18[7:0]							
$F9	USERDATA_19	USERDATA_19[7:0]							
$FA	USERDATA_1A	USERDATA_1A[7:0]							
$FB	USERDATA_1B	USERDATA_1B[7:0]							
$FC	USERDATA_1C	USERDATA_1C[7:0]							
$FD	USERDATA_1D	USERDATA_1D[7:0]							
$FE	USERDATA_1E	USERDATA_1E[7:0]							
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

6.2.41 CRC_UF2, CRC_F_A to CRC_F_F – lock and CRC registers (address $5F, $AF to $FF)

The lock and CRC registers are automatically programmed OTP registers which include the lock bit, the block identifier, and the block OTP array CRC use for error detection.

These registers are automatically programmed when the corresponding data array is programmed to OTP using the write OTP enable register as documented in Section 6.2.6 "WRITE_OTP_EN – write OTP enable register (address $11)".

Table 113. CRC_UF2, CRC_F_A to CRC_F_F – lock and CRC registers – (address $5F, $AF to $FF) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$5F	CRC_UF2	LOCK_UF2	0	0	0	CRC_UF2[3:0]			
Reset		0	0	0	0	0	0	0	0
$AF	CRC_F_A	LOCK_F_A	REGA_BLOCKID[2:0]			CRC_F_A[3:0]			
Reset		1	0	0	1	Varies			
$BF	CRC_F_B	LOCK_F_B	REGB_BLOCKID[2:0]			CRC_F_B[3:0]			
Reset		1	0	1	0	Varies			
$CF	CRC_F_C	LOCK_F_C	REGC_BLOCKID[2:0]			CRC_F_C[3:0]			
Reset		1	0	1	1	Varies			
$DF	CRC_F_D	LOCK_F_D	REGD_BLOCKID[2:0]			CRC_F_D[3:0]			
Reset		1	1	0	0	Varies			
$EF	CRC_F_E	LOCK_F_E	REGE_BLOCKID[2:0]			CRC_F_E[3:0]			
Reset		0	0	0	0	0	0	0	0
$FF	CRC_F_F	LOCK_F_F	REGF_BLOCKID[2:0]			CRC_F_F[3:0]			
Reset		0	0	0	0	0	0	0	0

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Table 114 shows the state of the lock bits, the block identifiers, and the CRC for each register block before and after programming.

Table 114. Register block before and after programming

Register block address	Lock bit bit[7]		Block identifier bit[6:4]		CRC bit[3:0]	
	Before programming	After programming	Before programming	After programming	Before programming	After programming
UF2	0	1	000	000	0000	Varies
$Ax	0	1	N/A	001	N/A	Varies
$Bx	0	1	N/A	010	N/A	Varies
$Cx	0	1	N/A	011	N/A	Varies
$Dx	0	1	N/A	100	N/A	Varies
$Ex	0	1	000	101	0000	Varies
$Fx	0	1	000	110	0000	Varies

6.2.42 Reserved registers

A register read command to a reserved register or a register with reserved bits will result in a valid response. The data for reserved bits may be 0 or 1.

A register write command to a reserved register or a register with reserved bits will execute and result in a valid response. The data for the reserved bits may be 0 or 1. A write to the reserved bits must always be '0' for normal device operation and performance.

6.2.43 Invalid register addresses

A register read command to a register address outside the addresses listed in Section 6.1 "User accessible data array" will result in a valid response. The data for the registers will be 00h.

A register write command to a register address outside the addresses listed in Section 6.1 "User accessible data array" will not execute, but will result in a valid response. The data for the registers will be 00h.

A register write command to a read-only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

6.3 OTP and read/write register array CRC verification

6.3.1 NXP OTP registers

The following registers are internal OTP registers. These registers are verified by the OTP ECC as well as an independent 4-bit CRC for each 16 byte block.

Table 115. Internal OTP registers

Memory type codes	
F	User-readable register with OTP

6.3.2 User OTP only registers

The following registers are internal OTP registers. These registers are verified by the OTP ECC as well as a 4-bit CRC for each 16 byte block. The CRC verification uses a generator polynomial of $g(x) = X^4 + X^3 + 1$, with a seed value = 0000. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

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Table 116. User OTP only registers

Memory type codes	
UF0	One-time user-programmable OTP Region 0
UF1	One-time user-programmable OTP Region 1

6.3.3 OTP modifiable registers

The following registers are user read/write registers as well as OTP registers with writable mirror registers. The OTP registers are verified by the OTP ECC as well as an independent 4-bit CRC stored in the CRC_UF2 register.

The values read from OTP can be overwritten while ENDINIT is not set. Once ENDINIT is set, the writable registers (all registers in the R/W and UF2 regions with the exception of the DEVLOCK_WR register) are verified by an additional continuous 4-bit CRC that is calculated on the entire array. The CRC verification uses a generator polynomial of $g(x) = X^4 + X^3 + 1$, with a seed value = 0000. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

Table 117. Registers verified by the OTP CRC

Memory type codes	
UF2	One-time user-programmable OTP Region 3 with modifiable mirror registers

Table 118. Registers verified by the ENDINIT calculated CRC

Memory type codes	
UF2	One-time user-programmable OTP Region 3 with modifiable mirror registers
R/W	User-writable register, with the exception of the DEVLOCK_WR register

6.4 Voltage regulators

The device derives its internal supply voltage from the V_{CC}/BUS_I and V_{SS} pins. The internal regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC, and supply dropouts on BUS_I. An external filter capacitor is required for V_{BUF}, as shown in Section 11.5 "DSI3 switch connected daisy chain mode ".

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the undervoltage detection thresholds. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below the undervoltage detection thresholds. A reference generator provides a reference voltage for the ΣΔ converter.

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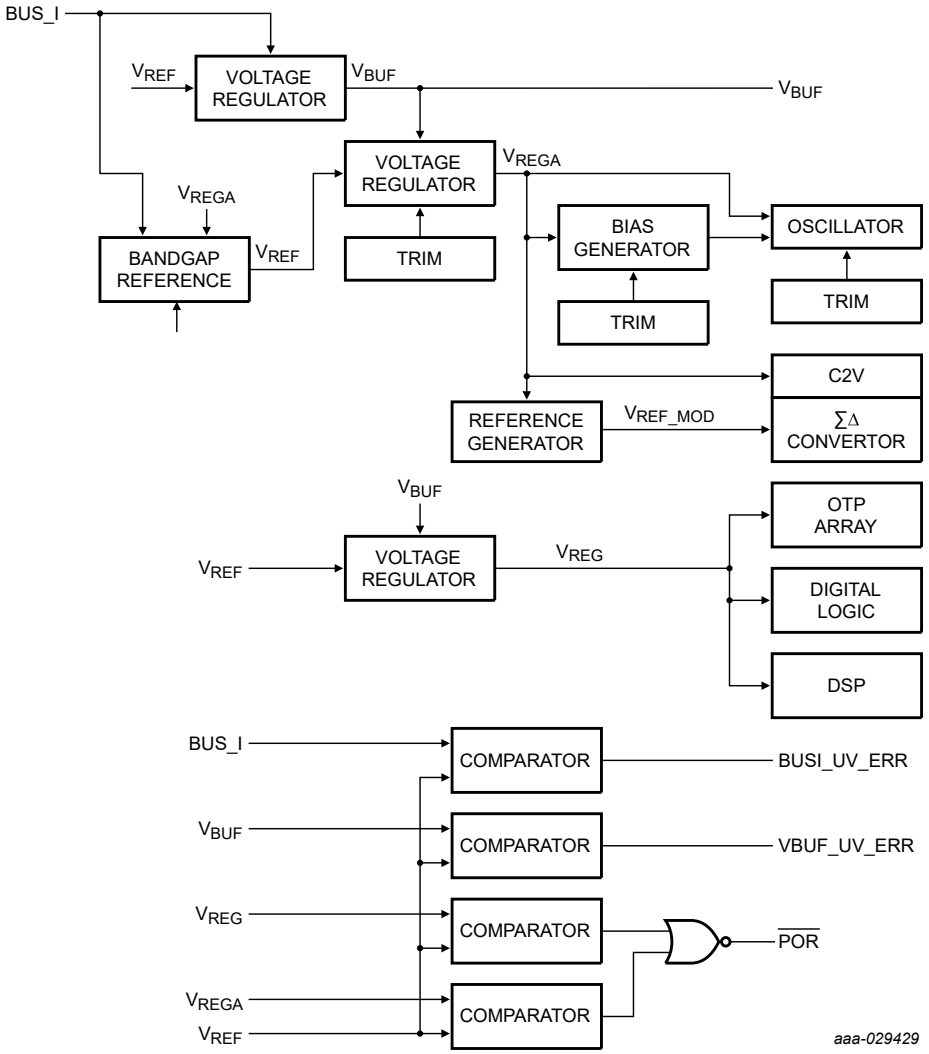


Figure 3. Voltage regulation and monitoring

6.4.1 V_{BUF} regulator capacitor and capacitor monitor

In DSI3 and PSI5 modes, the buffer regulator requires an external capacitor between the V_{BUF} pin and the V_{SS} pin. Section 11.5 "DSI3 switch connected daisy chain mode " shows the recommended types and values for each of these capacitors. A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF} capacitor becomes open. If the external capacitor is not present, the regulator voltage will fall below the threshold specified in Section 9 "Static characteristics" causing the VBUF_ERR bit to be set in the DEVSTAT1 register.

The V_{BUF} capacitor is tested synchronous to the protocol transmissions as shown in Figure 4, Figure 5, and Figure 6.

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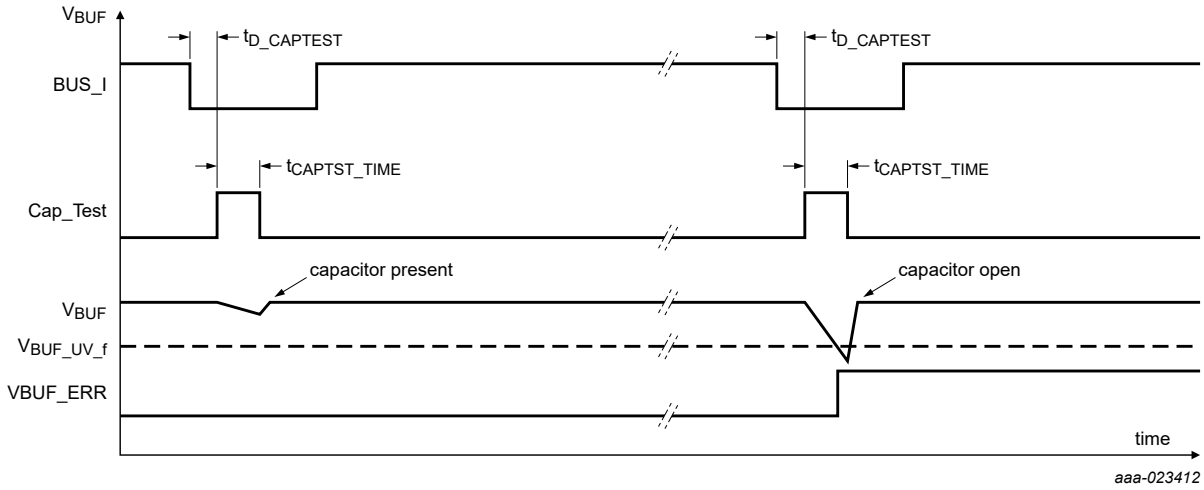


Figure 4. V_{BUF} capacitor monitor timing, DSI3

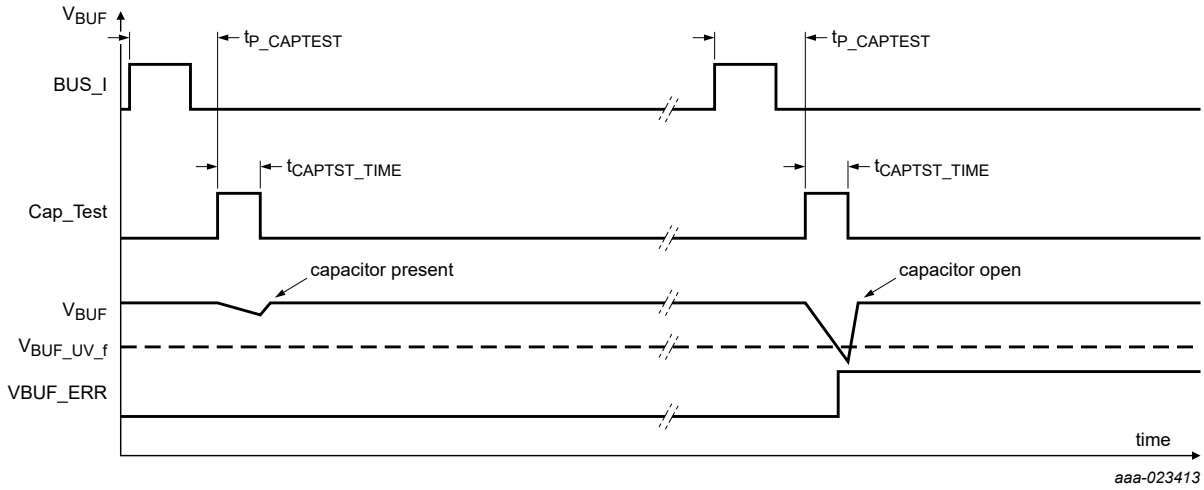


Figure 5. V_{BUF} capacitor monitor timing, PSI5 synchronous mode

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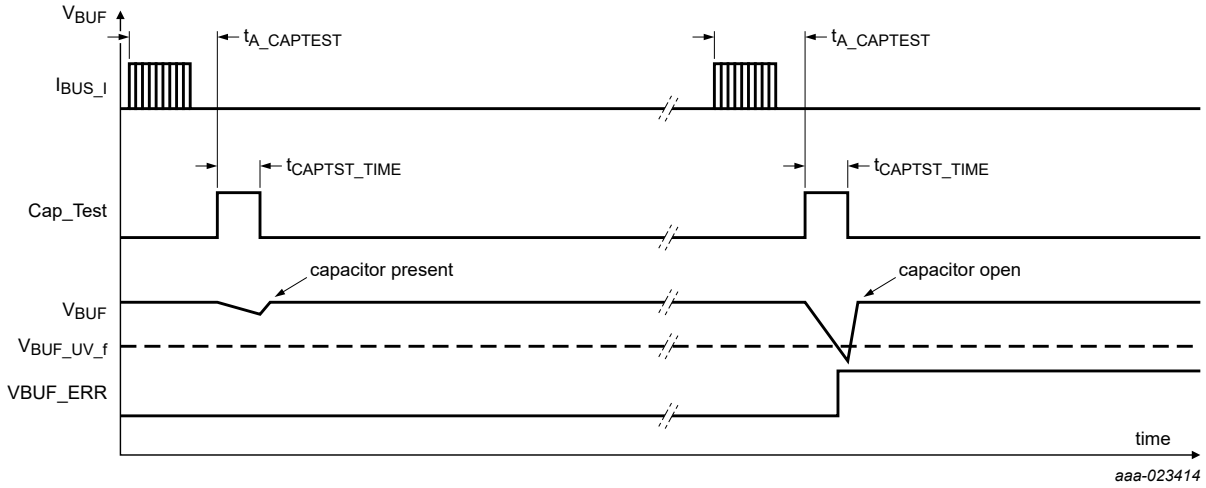


Figure 6. V_{BUF} capacitor monitor timing, PSI5 asynchronous mode

6.4.2 BUS_I, V_{BUF}, V_{REG}, V_{REGA}, undervoltage monitor

A circuit is incorporated to monitor the BUS_I supply voltage and the internally regulated voltages, V_{BUF}, V_{REG}, and V_{REGA}. If any of the voltages fall below the specified undervoltage thresholds in Section 9 "Static characteristics", the device reacts as follows:

- DSI3
  - If any supply falls below the specified threshold during a command transmission in command and response mode, the command is ignored, and no DSI3 response transmission occurs. Once the supply returns above the threshold, the device will resume decoding commands as specified in Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)".
  - If any supply falls below the specified threshold during a response transmission in command and response mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume decoding commands as specified in Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)".
  - If any supply falls below the specified threshold during a command transmission in periodic data collection mode, the command is ignored and no periodic response occurs during that period. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)". Any partially received background diagnostic mode command is flushed and the device will begin decoding a new background diagnostic mode command.
  - If any supply falls below the specified threshold during a periodic response transmission in periodic data collection mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)". Any partially received background diagnostic mode command is flushed and the device will begin decoding a new background diagnostic mode command.
  - If any supply falls below the specified threshold during a background diagnostic mode response transmission in periodic data collection mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands as specified in Section 6.2.2 "DEVSTATx – device status registers (address $01-

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$04)". Any partially received background diagnostic mode command is flushed and the device will begin decoding a new background diagnostic mode command.

- PSI5
  - If any supply falls below the specified threshold, PSI5 transmissions are terminated for the present response. Once the supply returns above the threshold, the device will resume responses as specified in Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)".

See Figure 7 for an example of a supply line interruption during a DSI3 or PSI5 response.

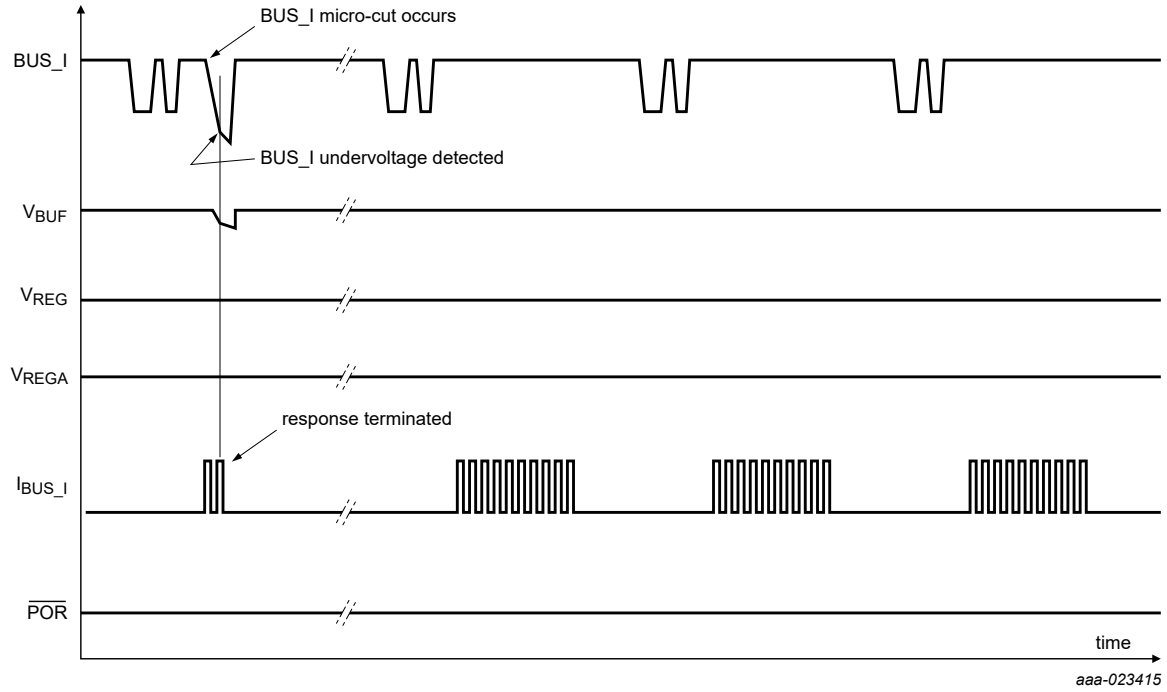


Figure 7. BUS_I micro-cut response (DSI3 or PSI5)

6.5 Internal oscillator

The device includes a factory trimmed oscillator as specified in Section 10 "Dynamic characteristics".

6.5.1 Oscillator training

The device includes a feature to train the oscillator to a tighter accuracy than the factory trimmed capability assuming the system master has a tighter oscillator accuracy than the slave factory trimmed capability. This feature can be enabled for DSI3 and PSI5 modes.

Note: *Oscillator training should not be used in systems that employ spread spectrum communication methods to reduce emissions.*

6.5.1.1 DSI3 oscillator training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the CRM_PER[1:0] and PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended periodic data collection mode command period into the PDCM_PER[2:0] bits and the intended command and response mode command period into the CRM_PER[1:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{CRM_PER_4ms_TYP}$ and $n_{PDCM_PER_4ms_TYP}$).

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In command and response mode, oscillator training is completed over 4 ms periods if and only if the CK_CAL_EN bit is set and the command and response mode period is between 500 µs and 4 ms, inclusive. The following procedure is used to train the oscillator (See Figure 8):

1. The device counts the number of oscillator cycles in $n_{CRM_PER_4ms_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC_4ms_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 10 "Dynamic characteristics", an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC_4ms_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target decreases by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC_4ms_TYP}$ – $OscTrain_{ADJ}$, the oscillator frequency target increases by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{CRM_PER_OSC}$ calculation.

If the CK_CAL_EN bit is cleared after oscillator training has already been initiated, the state of the oscillator is determined by the state of the CK_CAL_RST bit in the TIMING_CFG register. If the CK_CAL_RST bit is cleared, the last adjustment value for the oscillator is maintained. If the CK_CAL_RST bit is set, the oscillator is reset to its untrained value with the untrained tolerance specified in Section 10 "Dynamic characteristics".

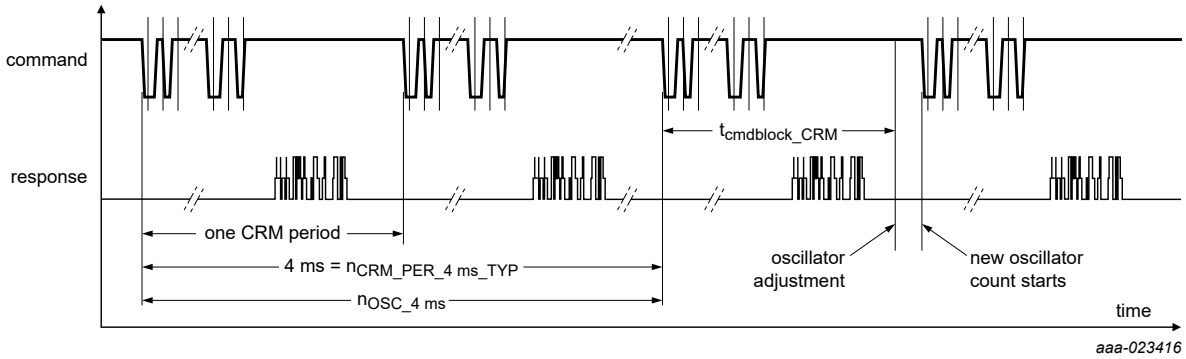


Figure 8. Command and response mode oscillator training timing diagram

In periodic data collection mode, oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator, see Figure 9:

1. The device counts the number of oscillator cycles in $n_{PDCM_PER_4ms_TYP}$ periods (n_{OSC_4ms}). n_{OSC_4ms} is compared to $n_{OSC_4ms_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 10 "Dynamic characteristics", an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC_4ms_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target decreases by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC_4ms_TYP}$ – $OscTrain_{ADJ}$, the oscillator frequency target increases by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM_PER_OSC}$ calculation.

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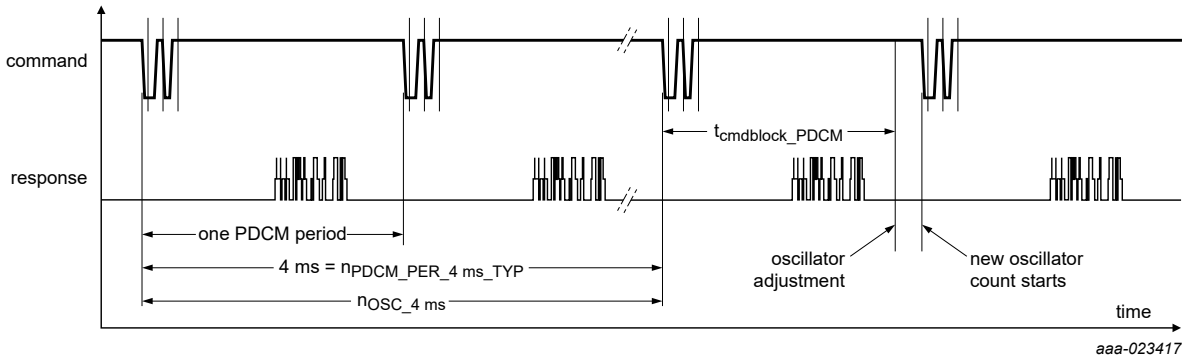


Figure 9. Periodic data collection mode oscillator training timing diagram

6.5.1.2 PSI5 oscillator training

Oscillator training is enabled if the CK_CAL_EN bit is set in the TIMING_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the PDCM_PER[2:0] bits of the user read/write register array. The sync pulse period is preprogrammed into the PDCM_PER[2:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{PSI5_PER_4ms_TYP}$).

Oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator (see Section 6.5.1.2 "PSI5 oscillator training"):

1. The device counts the number of oscillator cycles in $n_{PSI5_PER_4ms_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC_4ms_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in Section 10 "Dynamic characteristics", an oscillator adjustment is made. Otherwise, no adjustment is made.
   a. If n_{OSC_4ms} is greater than $n_{OSC_4ms_TYP}$ + $OscTrain_{ADJ}$, the oscillator frequency target decreases by $OscTrain_{RES}$.
   b. If n_{OSC_4ms} is less than $n_{OSC_4ms_TYP}$ – $OscTrain_{ADJ}$, the oscillator frequency target increases by $OscTrain_{RES}$.
   c. The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM_PER_OSC}$ calculation.

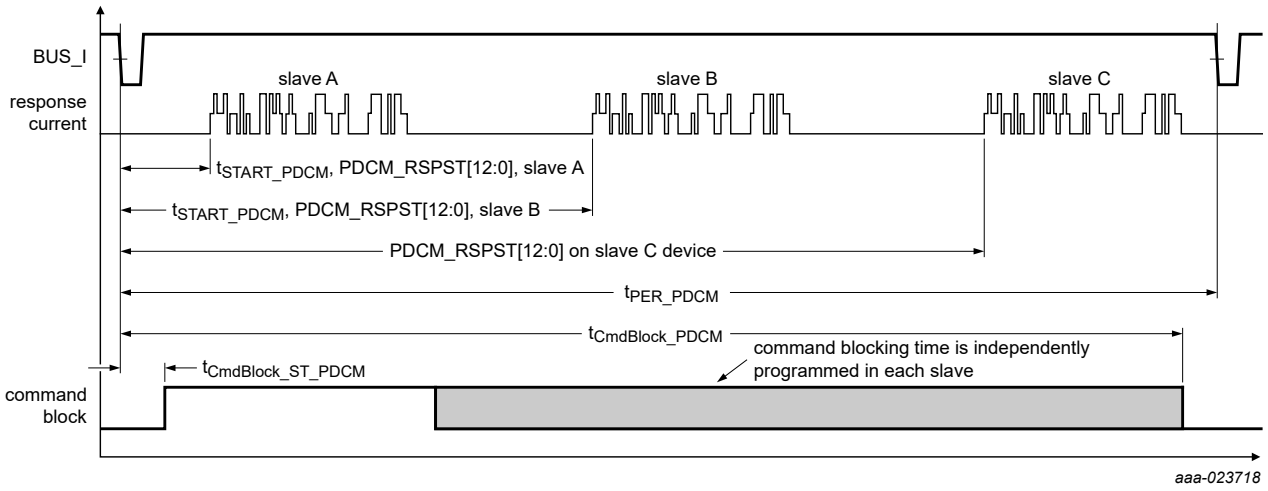


Figure 10. PSI5 oscillator training timing diagram

Note: *In order to benefit from the PSI5 oscillator training accuracy improvements, the oscillator must be trained prior to data transmissions in Initialization phase 2. For this reason, if oscillator training is enabled in PSI5*

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mode, the device will not respond to sync pulses during initialization phase 1, but oscillator training will be enabled t_{RS_PM} after reset.

6.5.2 Oscillator training error handling

If the user enables oscillator training, but the conditions are not correct to complete oscillator training, the OSCTRAIN_ERR bit is set in the DEVSTAT register. The following conditions will result in the OSCTRAIN_ERR bit being set.

- The CLK_CAL_EN bit in the TIMING_CFG register is set and the measured period (n_{OSC_4ms}) for any mode is outside the oscillator training window ($OscTrain_{WIN}$).
- The result of the comparison is filtered with an up and down counter.
- If n_{OSC_4ms} is outside the oscillator training window, the counter is incremented.
- If n_{OSC_4ms} is inside the oscillator training window, the counter is decremented.
- If the counter reaches 64 counts, the OSCTRAIN_ERR bit is set.
- The up and down counter has a maximum value of 127 and a minimum value of 0.
- The command and response mode period established by the PDCM_PER and CRM_PER settings does not fall within the 500 µs to 4 ms window.
- The command and response mode period established by the PDCM_PER and CRM_PER settings is not a whole number divisor of 4 ms.

6.6 Pressure sensor signal path

6.6.1 Transducer

See Section 9 "Static characteristics" and Section 10 "Dynamic characteristics" for transducer parameters.

6.6.2 Self-test functions

The device includes analog and digital self-test functions to verify the functionality of the transducer and the signal chain. The self-test functions are selected by writing to the ST_CTRL[3:0] bits in the DSP_CFG_U5 register. The ST_CTRL bits select the desired self-test connection as described below.

Once the ENDINIT bit is set, the ST_CTRL bits are forced to 0000. Future writes to the ST_CTRL bits are disabled until a device reset.

6.6.2.1 Startup P_{ABS} common mode verification

When the P_{ABS} common mode self-test is selected, the ST_ACTIVE bit is set, the ST_ERROR is cleared, and the device begins an internal measurement of the common mode signal of the P-cells and compares the result against a predetermined limit. If the result exceeds the limit, the ST_ERROR bit is set.

The P_{ABS} common mode self-test will repeat continuously every t_{ST_INIT} when the ST_CTRL bits are set to the specified value. Once the test is disabled, the ST_ERROR bit will be updated with the final test result within t_{ST_INIT} of disabling the test. The ST_ACTIVE bit will remain set until the final test result is reported. Figure 11 is an example of a user controlled self-test procedure:

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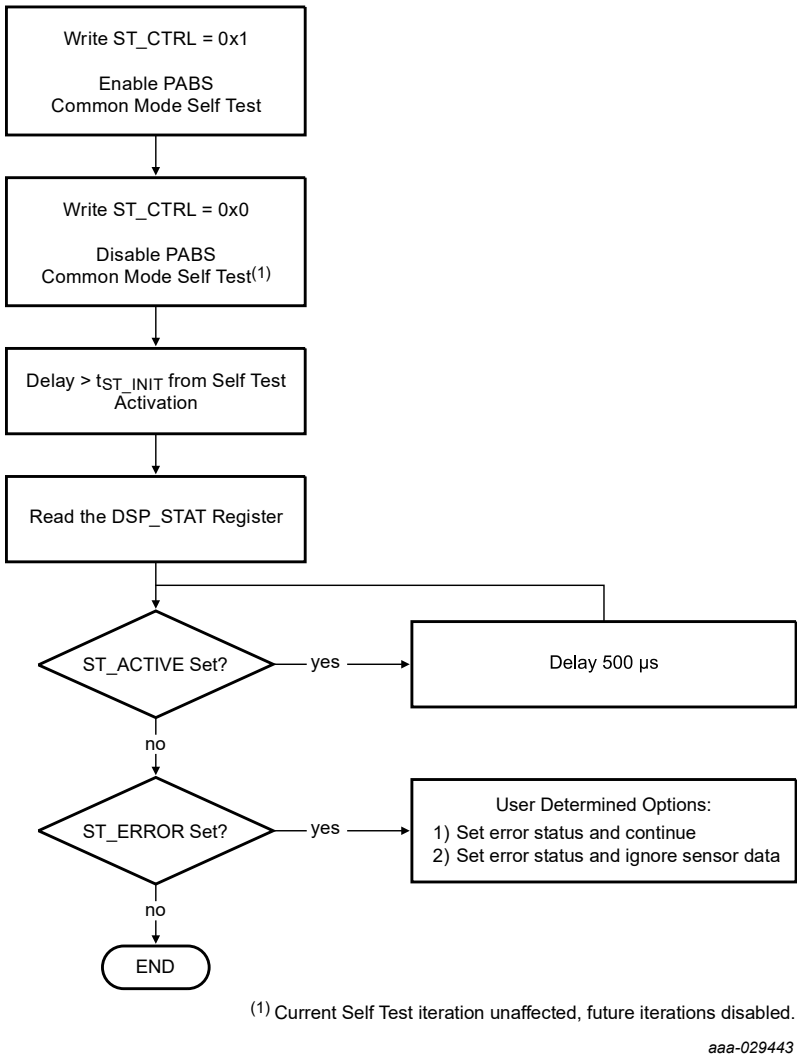


Figure 11. User-controlled PABS common mode self-test flowchart

6.6.2.2 Startup digital self-test verification

Four unique fixed values can be forced at the output of the sinc filter by writing to the ST_CTRL bits as shown in Table 119. The digital self-test values result in a constant value at the output of the signal chain. After a specified period of time, the SNS_DATAx register value can be verified against the values in Table 119. The values listed in Table 119 are only valid if the P_{ABS} signal is selected by the associated DATATYPEx bits. When any of these self-test functions are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 119. Startup digital self-test verification

ST_CTRL[3:0]				Function	SNS_DATAx register contents	
					Absolute pressure	Relative pressure
1	1	0	0	Digital self-test #1	8171h	8001h
1	1	0	1	Digital self-test #2	6C95h	8001h
1	1	1	0	Digital self-test #3	807Ah	8001h
1	1	1	1	Digital self-test #4	78ACh	8001h

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6.6.2.3 Startup sense data fixed value verification

Four unique fixed values can be forced to the SNS_DATAX_x registers by writing to the ST_CTRL bits as shown in Table 120. When any of these values are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 120. Startup sense data fixed value verification

ST_CTRL[3:0]				Function	SNS_DATAx register contents
0	1	0	0	DSP write to SNS_DATAx_X registers inhibited.	0000h
0	1	0	1	DSP write to SNS_DATAx_X registers inhibited.	AAAAh
0	1	1	0	DSP write to SNS_DATAx_X registers inhibited.	5555h
0	1	1	1	DSP write to SNS_DATAx_X registers inhibited.	FFFFh

6.6.2.4 PSI5 automatic startup self-test procedure

If the device is programmed to PSI5 mode, during PSI5 Initialization, the P_{ABS} common mode self-test, and digital self-test are run automatically. The test starts t_{PSI5ST_START} after POR. One iteration of the self-test is complete within t_{ST_INIT}. If the self-test fails, the self-test is repeated up to ST_RPT times. Once the test passes, or the maximum number of repeats has occurred, the ST_ACTIVE bit is cleared. If the test passes, the ST_ERROR bit is cleared. Otherwise, the ST_ERROR bit is set in the DSP_STAT register, the device will exit PSI5 initialization with a self-test error and transmit the self-test error message instead of sensor data. In this case, the ST_ERROR bit can only be cleared by a device reset.

After the self-test, the P0 filter startup is reset to the first phase and the filter is initialized for t_{ST_P0INIT}.

6.6.3 ΣΔ converter

A second order sigma delta modulator converts the transducer differential capacitance to a data stream that is input to the DSP. A simplified block diagram is shown in Figure 12.

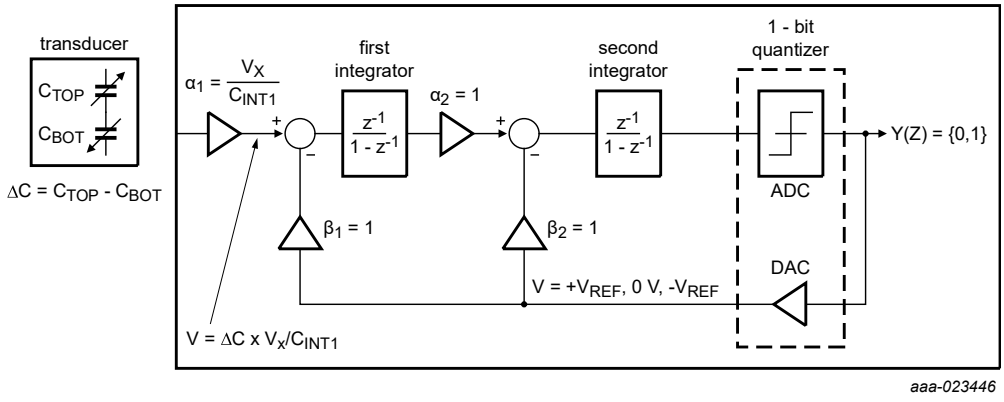


Figure 12. ΣΔ converter block diagram

The sigma delta modulator operates at a frequency of 1 MHz, with the following transfer function:

$$H(Z) = \frac{\alpha_1}{Z^2} \quad (2)$$

6.6.4 Digital signal processor

A digital signal processor (DSP) is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in Figure 13.

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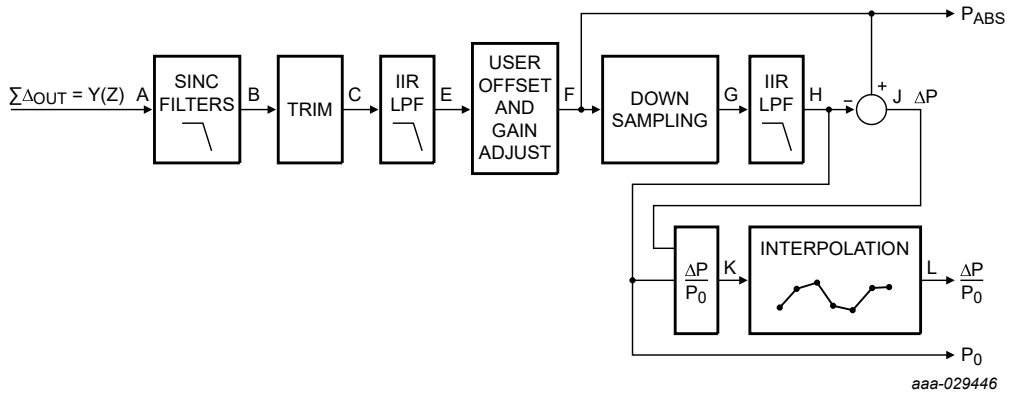


Figure 13. Signal chain diagram

Table 121. Digital signal processor details

Ref	Description	Sample time (µs)	Data width (bits)	Sign (bits)	Over range (bits)	Signal width (bits)	Signal margin (bits)	Typical block latency	Reference
A	ΣΔ	1	1	1	NA	1	NA	2.5 µs	Section 6.6.3 "ΣΔ converter"
B	SINC filters	48	23	1	NA	21	NA	48 µs	Section 6.6.4.1 "Decimation sinc filter"
C	Trim	48	32	1	2	18	11	NA	Section 6.6.4.2 "Signal trim and compensation"
E	Low-pass filter (P_{ABS})	48	32	1	2	18	11	Filter dependent	
F	User offset and gain adjust	48	32	1	2	18	11	NA	Section 6.2.25 "P_CAL_ZERO_x – pressure calibration registers (address $4C, $4D)"
G	Down sample	384	32	1	NA	31	NA	NA	Section 6.6.4.4 "P0 low-pass filter and gradient filter"
H	P_0 Low-pass filter	384	32	1	2	11	2	NA	Section 6.6.4.4 "P0 low-pass filter and gradient filter"
J	ΔP	48	32	1	2	11	2	NA	Section 6.6.4.5 "ΔP/P0 calculation"
K	$\Delta P/P_0$	48	26	1	2	11	2	NA	Section 6.6.4.5 "ΔP/P0 calculation"
L	Interpolation ($\Delta P/P_0$ Only)	3	24	1	1	18	3	tsigchainxx	Section 6.6.4.6 "Data interpolation"

6.6.4.1 Decimation sinc filter

The output of the ΣΔ modulator is decimated and converted to a parallel value by one 3rd order sinc filter with a decimation ratio of 48.

$$H(Z) = \left(\frac{1}{48^3}\right) \times \left(\frac{1-Z^{-48}}{1-Z^{-1}}\right)^3 \quad (3)$$

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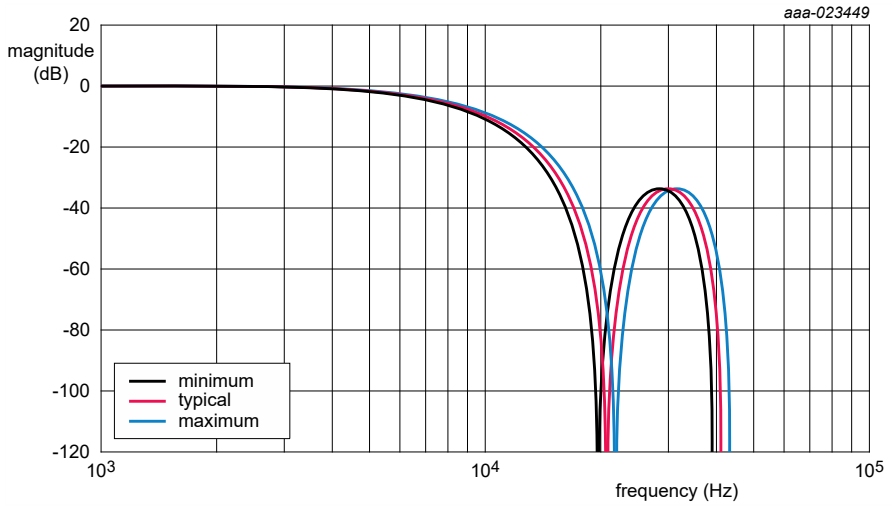


Figure 14. Sinc filter response

6.6.4.2 Signal trim and compensation

The device includes digital trim to compensate for sensor offset, sensitivity, and nonlinearity over temperature. The following equation is used for the trim compensation:

$$Trim_{OUT} = P_0 + P_P \cdot Trim_{In} + P_{PP} \cdot Trim_{In}^{\ 2} + P_{PPP} \cdot Trim_{In}^{\ 3} + P_t \cdot (T - T_{25}) + P_{tt} \cdot (T - T_{25})^2 + P_{pt} \cdot Trim_{In} \cdot (T - T_{25}) \quad (4)$$

Table 122. Signal trim and compensation

Variable name	Description
P_0	Offset compensation
P_P	Sensitivity compensation
P_{PP}	Linearity compensation
P_{PPP}	3rd order compensation
P_t	Offset compensation with first order temperature compensation
P_{tt}	Offset compensation with second order temperature compensation
P_{Pt}	Sensitivity compensation with first order temperature compensation
T	Temperature sensor digital output value
T_{25}	Temperature sensor output value stored at the ambient test insertion
$Trim_{In}$	Output of the sinc filter
$Trim_{Out}$	Output of the trim block

6.6.4.3 Low-pass filter

Data from the sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{21} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})} \quad (5)$$

The filter coefficients are selected with the LPF[3:0] bits in the DSP_CFG_U1 registers.

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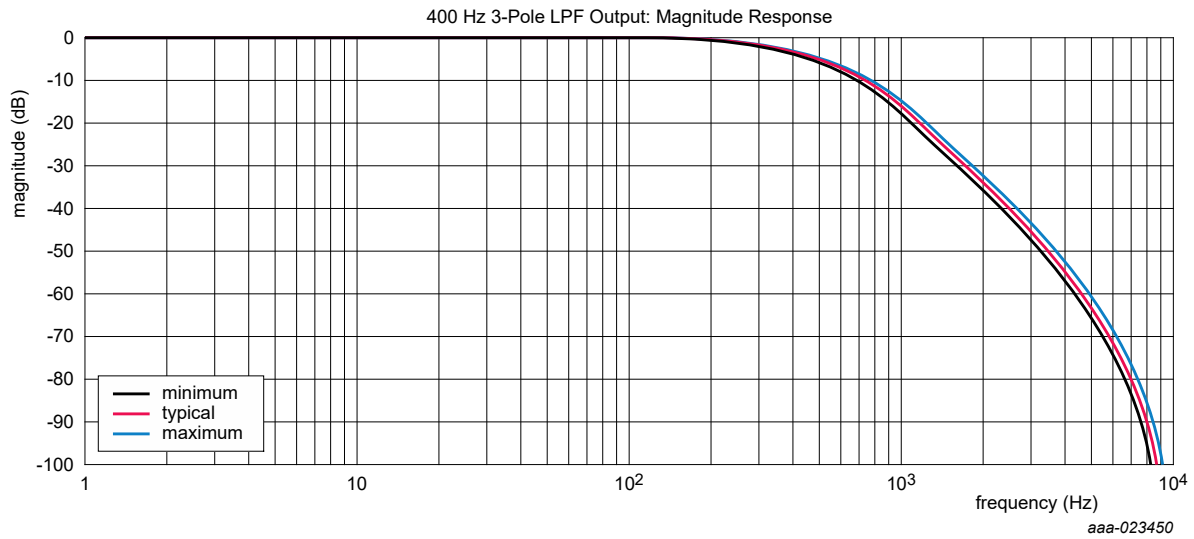
The filter selection options are listed in Section 6.2.20 "DSP_CFG_U1 – DSP user configuration #1 register (address $40)". Response parameters for the low-pass filter are specified in Section 10 "Dynamic characteristics". Filter characteristics for the highest sample rate are illustrated in the following figures.

Table 123. Low-pass filter options

Filter number	Typical –3 dB frequency	Filter order	Filter coefficients (24-bit)				Group delay (µs)	Typical attenuation @ 1000 Hz (dB)
0	370 Hz	2	a_0	0.017940729763385	—	—	585.6	14.1
			n_{11}	0.249999999999997	d_{11}	1		
			n_{12}	0.499999999999994	d_{12}	–1.763648824568436		
			n_{13}	0.250000000000003	d_{13}	0.781589554331821		
			n_{21}	1	d_{21}	1		
			n_{22}	0	d_{22}	0		
			n_{23}	0	d_{23}	0		
1	400 Hz	3	a_0	0.148157329921697	—	—	697.4	16.7
			n_{11}	0.013516264115488	d_{11}	1		
			n_{12}	0.013519651938257	d_{12}	–0.851842670078304		
			n_{13}	0	d_{13}	0		
			n_{21}	0.250031330983387	d_{21}	1		
			n_{22}	0.499999992148175	d_{22}	–1.749563460775225		
			n_{23}	0.249968676868576	d_{23}	0.776599376828971		
2	800 Hz	4	a_0	0.088642612609670	—	—	418	4.95
			n_{11}	0.029638050039039	d_{11}	1		
			n_{12}	0.059333280736160	d_{12}	–1.422792640957290		
			n_{13}	0.029695285913601	d_{13}	0.511435253566960		
			n_{21}	0.250241278804809	d_{21}	1		
			n_{22}	0.499999767379068	d_{22}	–1.503329908017845		
			n_{23}	0.249758953816089	d_{23}	0.621996524706640		
3	1000 Hz	4	a_0	0.129604264748411	—	—	333	2.99
			n_{11}	0.043719804402508	d_{11}	1		
			n_{12}	0.087543281056143	d_{12}	–1.300502656562698		
			n_{13}	0.043823599710731	d_{13}	0.430106921311110		
			n_{21}	0.250296586927511	d_{21}	1		
			n_{22}	0.499999648540934	d_{22}	–1.379959571988366		
			n_{23}	0.249703764531484	d_{23}	0.555046257157745		

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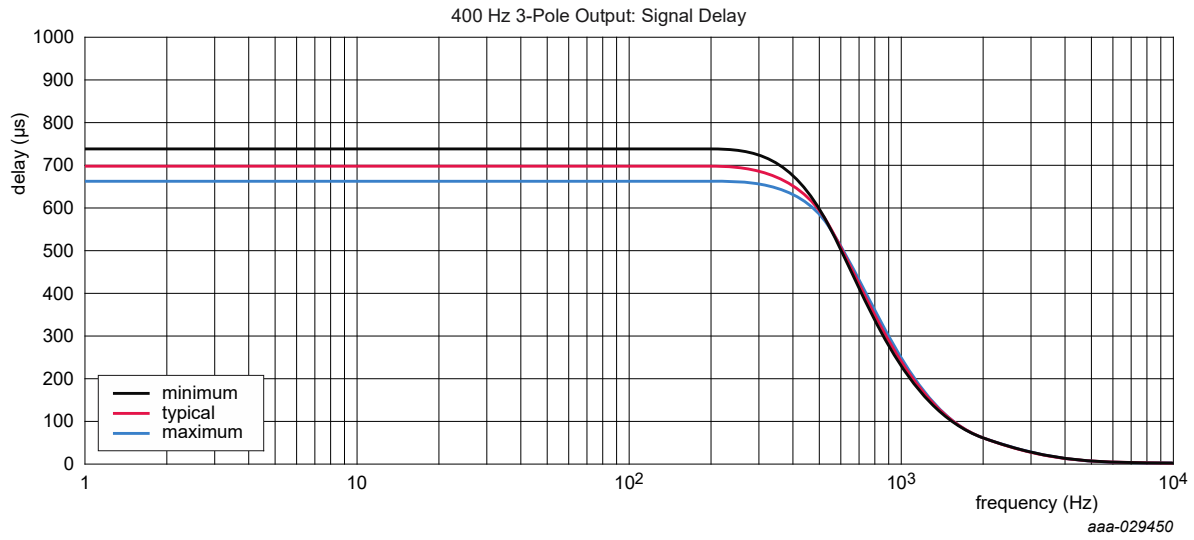


Figure 15. 400 Hz, 3-pole low-pass filter response

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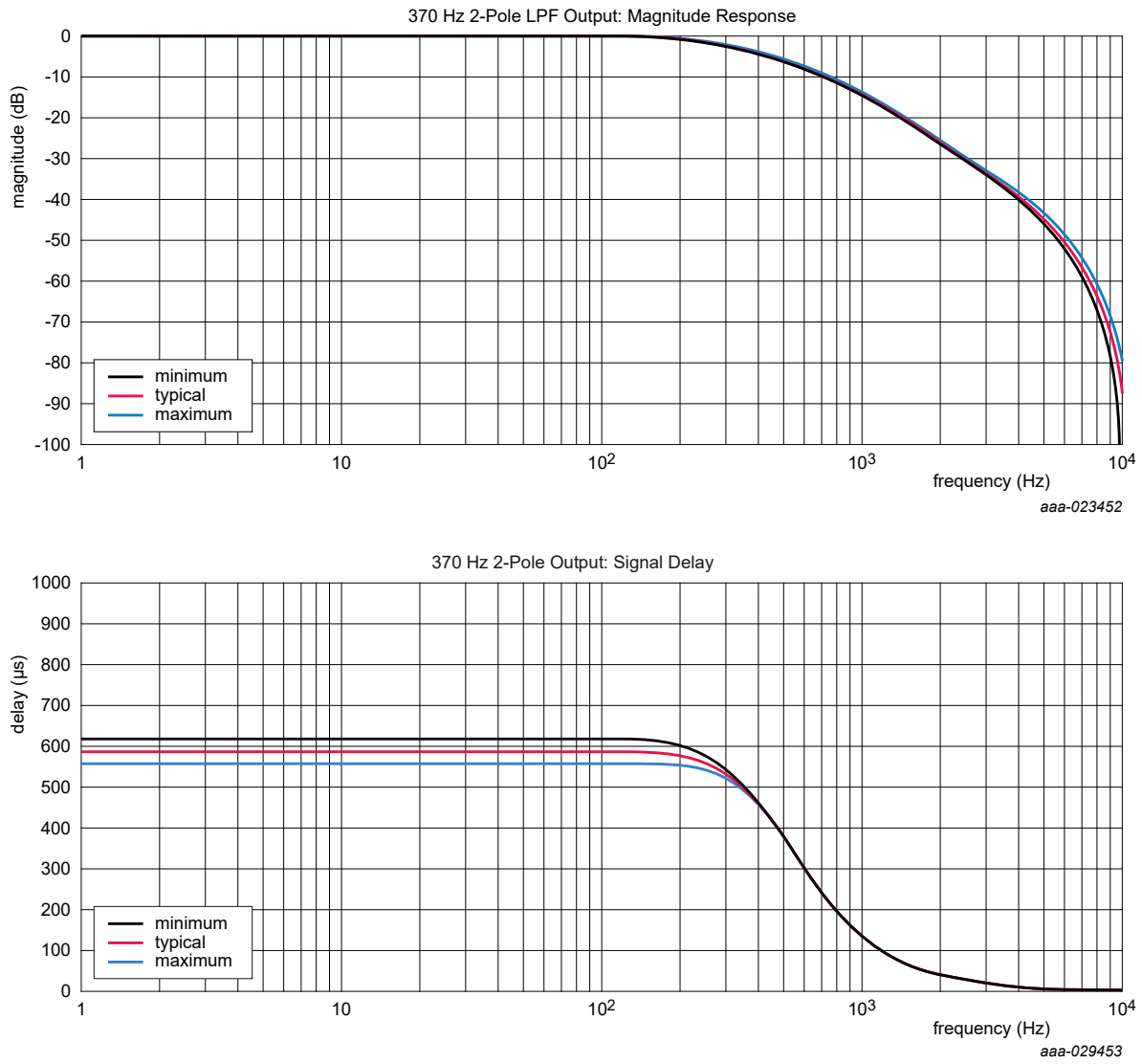
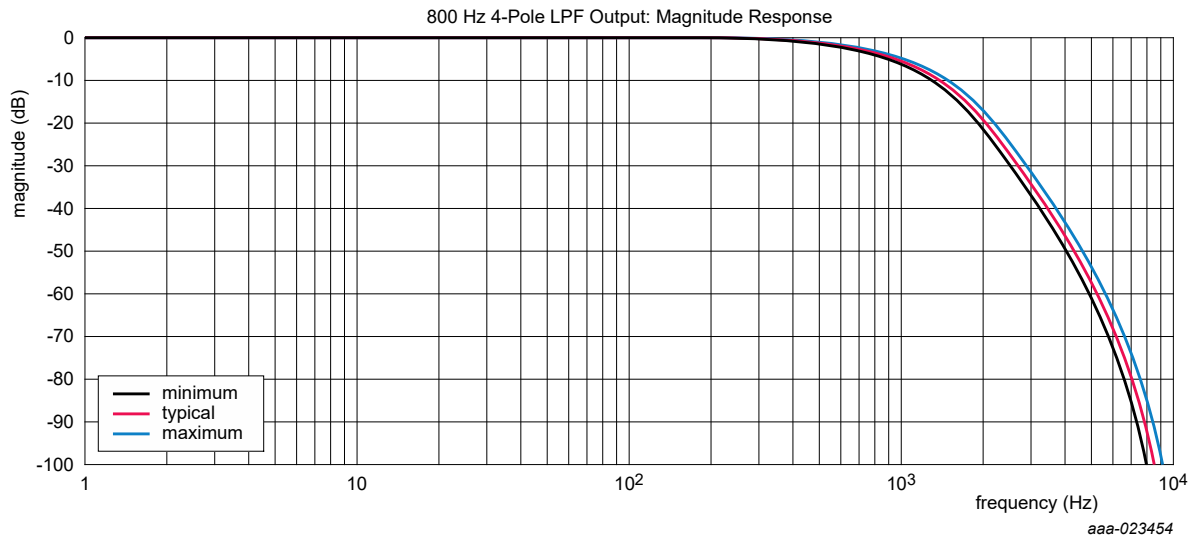


Figure 16. 370 Hz, 2-pole low-pass filter response

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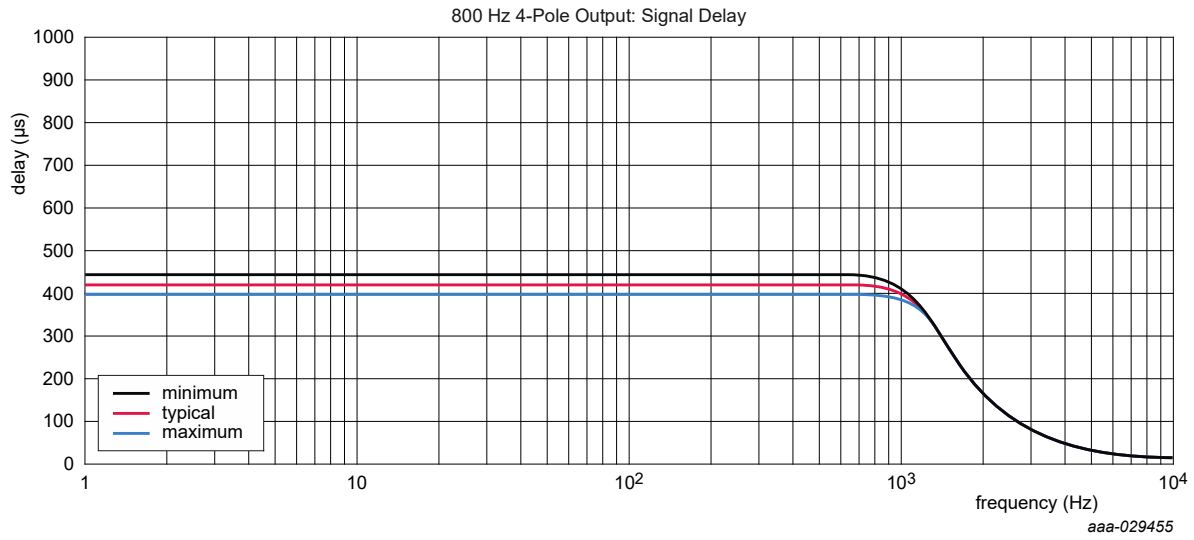
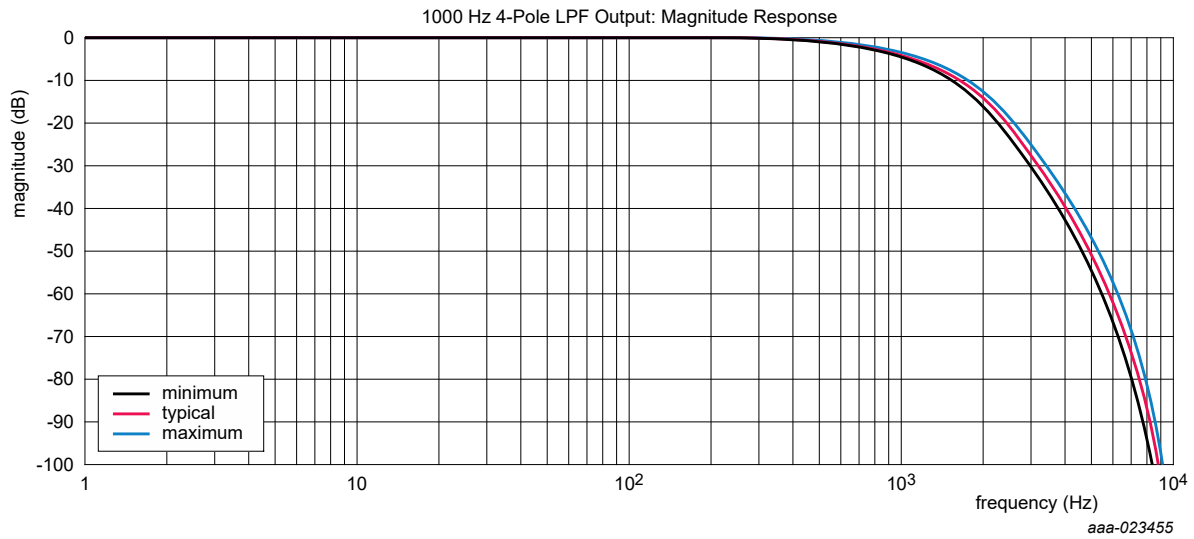


Figure 17. 800 Hz, 4-pole low-pass filter response

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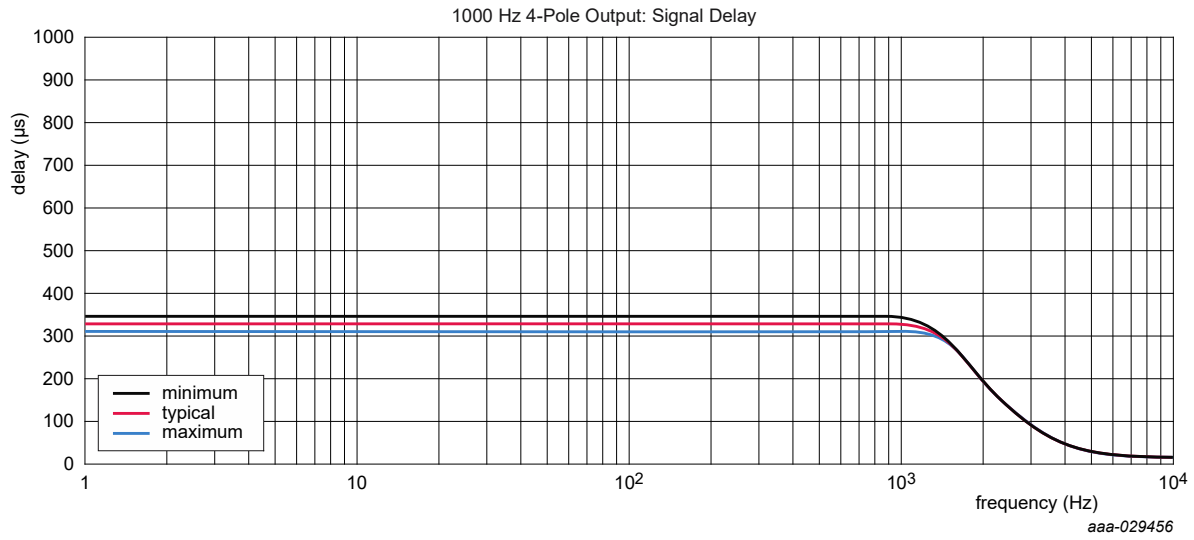


Figure 18. 1000 Hz, 4-pole low-pass filter response

6.6.4.4 P_0 low-pass filter and gradient filter

The device provides a low-pass filter to provide an average absolute pressure value called P_0. A block diagram of the P_0 filter is shown in Figure 19.

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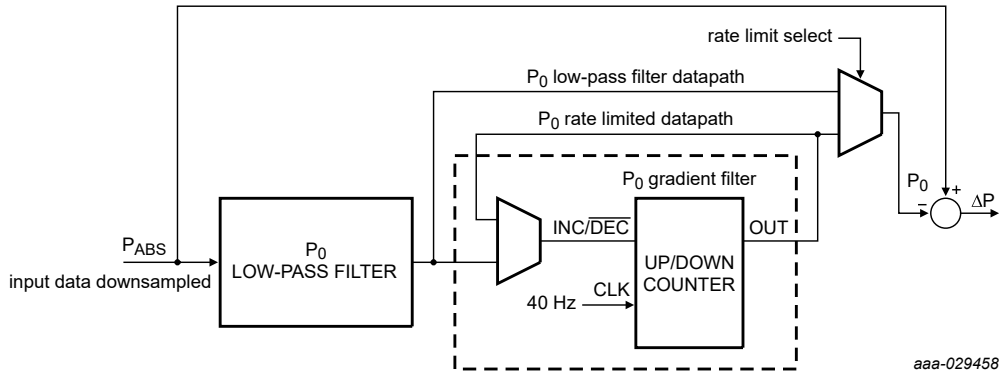


Figure 19. P_0 low-pass filter block diagram

Equation 6 applies to the low-pass filter block shown in Figure 19.

$$\frac{n_0}{1-(d_1 \cdot z^{-1})} \tag{6}$$

The transfer function of the offset low-pass filter is:

$$H(z) = a_0 \times \frac{n_0 + (n_1 \cdot z^{-1})}{d_0 + (d_1 \cdot z^{-1})} \tag{7}$$

Response parameters are specified in Section 7 "Limiting values" and the P_0 low-pass filter coefficients are specified in Table 124.

During startup, multiple phases of the P_0 low-pass filter are used to allow for fast convergence of the absolute pressure value during initialization. The rate limiting is also bypassed regardless of the state of the P0_RLD bit in the DSP_CFG_U4 register. The low-pass filter details and timing for the startup phases is shown in Table 124.

Table 124. Low-pass filter details and timing for the startup phases

P_0 LPF startup phase	Time from reset to start of phase (ms)	Sample time (us)	Coefficients (24-bit)				LPF corner frequency (–3 dB) (Hz)	Time constant (τ) (ms)	Rate limiting
0	0	384	a0	0.333703567338226			163.8	0.9714	Bypassed
			n0	0.5	n1	0.5			
			d0	1.0	d1	–0.666296432661774			
1	4.096	384	a0	0.094245715384814			40.96	3.886	Bypassed
			n0	0.5	n1	0.500000000000001			
			d0	1.0	d1	–0.905754284615186			
2	8.192	384	a0	0.024406235232995			10.24	15.54	Bypassed
			n0	0.5	n1	0.499999999999995			
			d0	1.0	d1	–0.975593764767005			
3	24.58	384	a0	0.006157625397102			2.560	62.17	Bypassed
			n0	0.5	n1	0.5			
			d0	1.0	d1	–0.993842374602898			
4	90.11	384	a0	0.001542964638922			0.6400	248.7	Bypassed
			n0	0.5	n1	0.5			
			d0	1.0	d1	–0.998457035361078			

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Table 124. Low-pass filter details and timing for the startup phases...*continued*

P_0 LPF startup phase	Time from reset to start of phase (ms)	Sample time (us)	Coefficients (24-bit)				LPF corner frequency (–3 dB) (Hz)	Time constant (τ) (ms)	Rate limiting
5	352.3	384	a0	0.000385964411427			0.1600	994.7	Controlled by P0_RLD
			n0	0.49999988079071	n1	0.49999988079071			
			d0	0.000385964411427	d1	–0.999614035588573			
6	1401	384	a0	0.000385964411427			0.1600	994.7	Controlled by P0_RLD
			n0	0.49999988079071	n1	0.49999988079071			
			d0	1.0	d1	–0.999614035588573			
Self-test Active	Output Frozen								

Note: *When rate limiting is disabled, the output of the rate limiting is set to the output of the P_0 low-pass filter.*

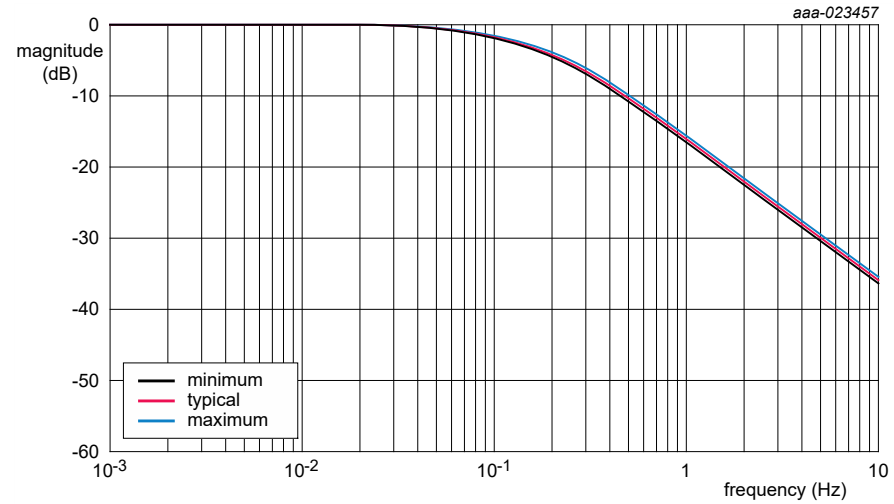


Figure 20. 0.16 Hz, 1-Pole P_0 low-pass filter response

6.6.4.5 ΔP/P_0 calculation

The device includes a ΔP/P_0 calculation based on Equation 8:

$$\Delta P / P_0 = \frac{P_{ABS} - P_0}{P_0} \tag{8}$$

The ΔP/P_0 output data equations for all ranges are in Section 6.6.4.7 "Output scaling equations". The range of the ambient pressure, absolute pressure for each ΔP/P_0 range is shown in Section 6.6.4.5 "ΔP/P0 calculation".

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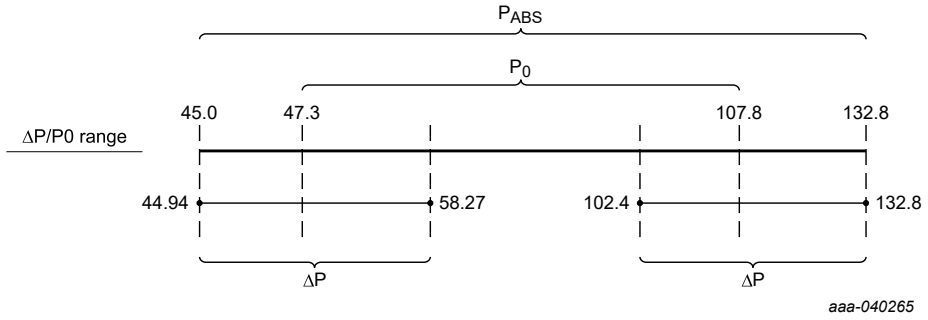


Figure 21. P_0 and P_{ABS} range

6.6.4.6 Data interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. Transmitted data is interpolated from the two previous samples, resulting in a latency of one sample time, and a maximum signal jitter of 1/16 of the sample time. The device uses the following equation for calculating the interpolation:

$$DataInterpOut_i = DataInterpOut_{i-1} + \frac{DSPOut_{Current} - DataInterpOut_{i-1}}{16-(i-1)} \quad (9)$$

$$DataInterpOut_0 = DSPOut_{Previous} \quad (10)$$

An example of the output interpolation is shown in Figure 22.

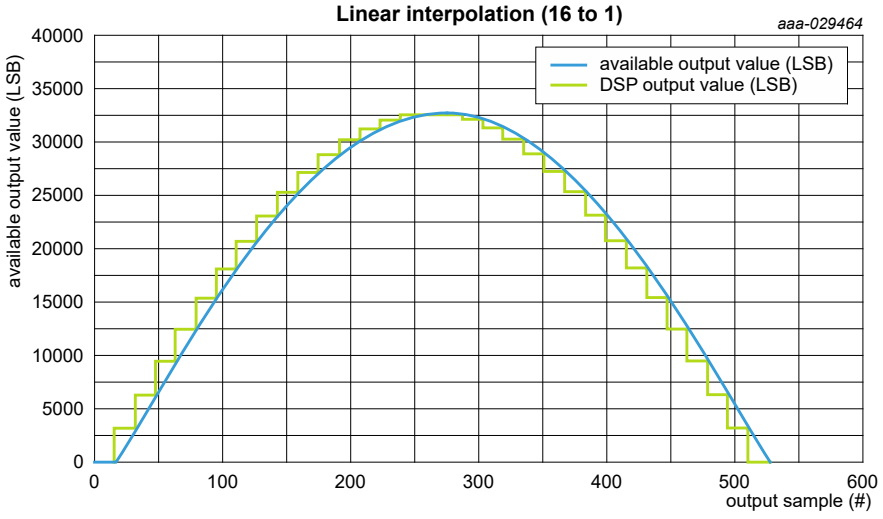


Figure 22. Output interpolation example

6.6.4.7 Output scaling equations

6.6.4.7.1 Absolute pressure scaling equation

Equation 11 is used to convert absolute pressure readings with the variables as specified in Table 125.

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Note: *The specified values apply only if the P_CAL_ZERO value is set to 0000h.*

$$PABS_{kPa} = \frac{PABS_{LSB} - PABSOFF_{LSB}}{PABS_{SENSE}} \quad (11)$$

Where:

$PABS_{kPa}$ = The absolute pressure output in kPa

$PABS_{LSB}$ = The absolute pressure output in LSB

$PABSOFF_{LSB}$ = The absolute pressure output value at 0 kPa in LSB

$PABS_{SENSE}$ = The expected absolute pressure sensitivity in LSB/kPa = 28.75LSB/KPa

Table 125. Absolute pressure readings variables

Data reading	$PABSOff_{LSB}$ (LSB)	$PABS_{SENSE}$ (LSB/kPa)
16-bit register read	28672	57.5
16-bit DSI3 PDCM data	28672	57.5
12-bit DSI3 PDCM data	0	28.75
12-bit PSI5 sensor data (Initialization phase 3)	0	28.75
10-bit DSI3 PDCM data	0	7.188
Interrupt threshold registers	28672	57.5
P Zero calibration registers	0	57.5

6.6.4.7.2 Relative pressure scaling equation

Equation 12 is used to convert relative pressure readings with the variables as specified in Table 126.

Note: *The specified values apply only if the P_CAL_ZERO value is set to 0000h.*

$$PREL_{PERCENT} = \frac{PREL_{LSB} - PREL0_{LSB}}{PREL_{SENSE}} \quad (12)$$

Where:

$PREL_{PERCENT}$ = The relative pressure output in percent

$PREL_{LSB}$ = The relative pressure output in LSB

$PREL0_{LSB}$ = The expected relative pressure output in LSB at constant pressure

$PREL_{SENSE}$ = The expected relative pressure sensitivity in LSB/%

Table 126. Relative pressure readings variables

Data reading	$PREL0_{LSB}$ (LSB)	$PREL_{SENSE}$ (LSB/%)
16-bit register read	30144	240
16-bit DSI3 PDCM data	30144	240
12-bit DSI3 PDCM data	736	120
10-bit DSI3 PDCM data	184	30

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Table 126. Relative pressure readings variables...*continued*

Data reading	$PREL0_{LSB}$ (LSB)	$PREL_{SENSE}$ (LSB/%)
10-bit PSI5 data	–328	30

6.6.5 Temperature sensor

6.6.5.1 Temperature sensor signal chain

The device includes a temperature sensor for signal compensation and user readability. A simplified block diagram is shown in Figure 23. Temperature sensor parameters are specified in Section 9 "Static characteristics" and Section 10 "Dynamic characteristics".

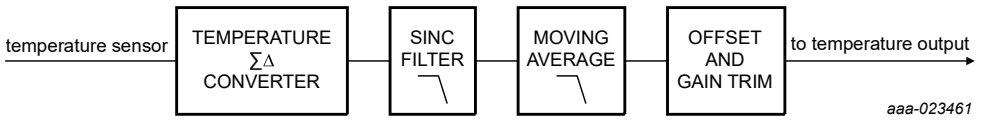


Figure 23. Temperature sensor signal chain block diagram

6.6.5.2 Temperature sensor output scaling equations

Equation 13 is used to convert temperature readings with the variables as specified in Table 127:

$$T_{DEGC} = \frac{T_{LSB} - T0_{LSB}}{T_{SENSE}} \quad (13)$$

Where:

T_{DEGC} = The temperature output in degrees C

T_{LSB} = The temperature output in LSB

$T0_{LSB}$ = The expected temperature output in LSB at 0 °C

T_{SENSE} = The expected temperature sensitivity in LSB/C

Table 127. Conversion variables

Data reading	$T0_{LSB}$ (LSB)	T_{SENSE} (LSB/C)
8-bit register read	68	1
16-bit register read	17408	256
16-bit DSI3 PDCM data	17408	256
12-bit DSI3 PDCM data	1088	16
10-bit DSI3 PDCM data	272	4
10-bit PSI5 data	–27	1

6.6.6 Common mode error detection signal chain

The device includes a startup pressure transducer common mode error detection. A simplified block diagram is shown in Figure 24. The startup common mode self-test is conducted as described in Section 6.6.2.1 "Startup PABS common mode verification".

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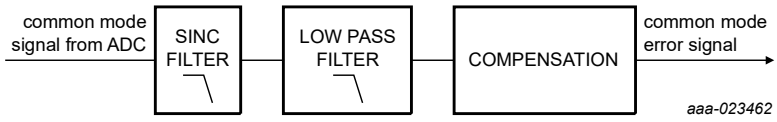


Figure 24. Common mode error detection signal chain block diagram

6.7 Pressure sensor accuracy (drift over temperature and life)

The absolute pressure accuracy is specified in Figure 25 and Figure 26.

Figure 25 shows the absolute pressure drift over the entire specified temperature range. The absolute pressure drift over temperature is guaranteed by production testing.

Figure 26 shows a multiplying factor that accounts for the life time drift of the pressure sensor. The results in Figure 26 have been obtained by qualification testing to conform to the AEC-Q100[4] standards.

As an example, at room temperature, the worst case drift that the pressure sensor might have after accounting for lifetime performance is (1 kPa × multiplying factor) = 2 kPa.

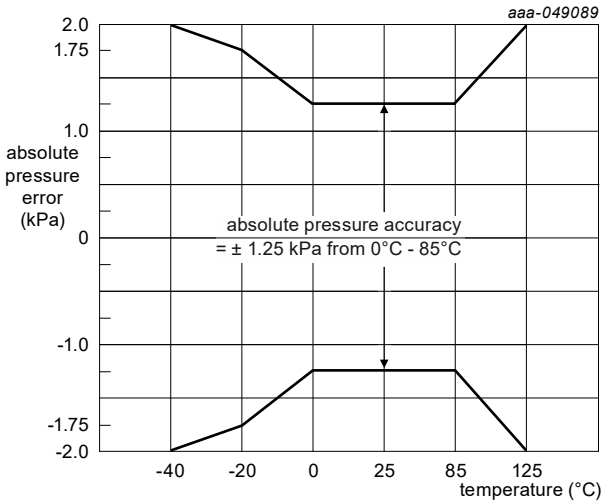


Figure 25. Absolute pressure accuracy as a function of temperature

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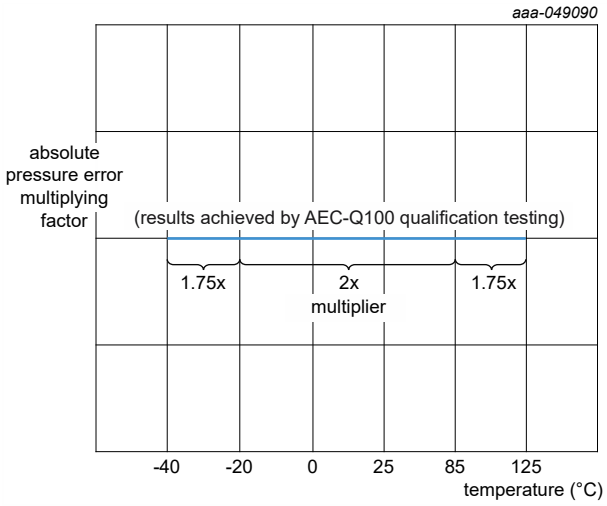


Figure 26. Absolute pressure accuracy multiplier over life

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7 Limiting values

Limiting values specify the absolute minimum and maximum ratings of the product, beyond which the product may be damaged or the lifetime may be reduced.

Table 128. Limiting values

Symbol	Parameter	Conditions	Value	Unit
BUS_I_{REV}	Supply voltage (BUS_I/V_{CC}, BUS_O, BUSSW_H)	Reverse current externally limited to ≤ 160 mA, t ≤ 80 ms [1]	–0.7	V
BUS_I_{MAX}		Continuous [1]	+20.0	V
VBUFMAX	V_{BUF}	[1]	–0.3 to +7.0	V
VIOMAX	BUSSW_L	[1]	–0.3 to V_{BUF} + 0.3	V
I_{SUPMAX}	BUS_I/V_{CC} and BUS_O continuous current	[1]	200	mA
g_{shock}	Unpowered shock (six sides, 0.5 ms duration)	[2]	±2000	g
g_{shock}	Unpowered shock (six sides, 0.5 ms duration)	[3]	±5000	g
h_{DROP}	Drop shock (to concrete, tile or steel surface, 10 drops, any orientation)	[2]	1.2	m
V_{ESD}	Electrostatic discharge (per AEC-Q100), external pins	BUS_I/V_{CC}, BUS_O, BUSRTN, HBM (100 pF, 1.5 kΩ) [2]	±4000	V
V_{ESD}	Electrostatic discharge (per AEC-Q100)	HBM (100 pF, 1.5 kΩ) [2]	±2000	V
V_{ESD}		CDM (R = 0 Ω) [2]	±750	V
T_{stg}	Temperature range	Storage [2]	–40 to +125	°C
T_J		Junction [4]	–40 to +150	°C
p_{MAX}	Maximum absolute pressure	Continuous (Pressure applied for 1 hour continuously at room temperature and no bias) [2]	420	kPa
p_{BURST}		Burst (tested at 100 ms) [2]	420	kPa
p_{MIN}	Minimum absolute pressure	Continuous [2]	15	kPa
f_{SEAL}	Pressure sealing force applied to top face of package	[2]	10	N
θ_{JA}	Thermal resistance	[4] [5]	120	°C/W

[1] Functionality verified by characterization.
[2] Parameter verified by qualification testing.
[3] Parameter verified by functional evaluation.
[4] Functionality verified by modeling, simulation and/or design verification.
[5] Thermal resistance provided with device mounted to a two-layer, 1.6 mm FR-4 PCB as documented in AN1902 with one signal layer and one ground layer.

8 Recommended operating conditions

Table 129. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HIGH}	DSI3 supply voltage (V_{HIGH})	Measured at BUS_I [1]	—	—	20.0	V
V_{LOW}	DSI3 supply voltage (V_{LOW})	Measured at BUS_I [1]	4.0	—	—	V
V_{PSI5}	PSI5 supply voltage (excluding sync pulse)	— [1]	4.2	—	16.0	V
$V_{BUS_I_UV}$	Supply voltage (undervoltage)	— [1]	$V_{BUS_I_UV_F}$	—	V_{LOW_min}	V
V_{PP}	Programming voltage	Applied to BUS_I, (I_{PP} ≤ 5 mA, T_A= 29 °C) [2]	9.0	10.0	11.0	V
$V_{BUS_I_ESD}$	ESD operating voltage (no device reset, C_{BUS_IN} = 220 pF)	Maximum ±15 kV air discharge, 330 pF, 2.0 kΩ [2] [3]	—	—	10.0	V
T_A	Operating temperature range	Production tested operating temperature range [1]	–20 (T_L)	—	+85 (T_H)	°C
T_A		Guaranteed operating temperature range [4]	–40 (T_L)	—	+125 (T_H)	°C
$V_{CC_RAMP_SAT}$	Supply power on ramp rate	[2]	0.00001	—	10	V/µs

[1] Parameter verified by final test.
[2] Parameter verified by functional evaluation.
[3] Functionality verified by modeling, simulation and/or design verification.
[4] Parameter verified by qualification testing.

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9 Static characteristics

$V_{BUS_I_L_min} \le (V_{BUS_I} - V_{SS}) \le V_{BUS_I_H_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Table 130. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply and I/O						
I_{q_4}	Quiescent supply current	V_{BUS_I} = 4 V [1]	4.0	—	8.0	mA
I_{q_20}		V_{BUS_I} = 20 V [1]	4.0	—	8.0	mA
$I_{R_DSI_1}$	Response current	DSI low [1]	I_q + 10.5	I_q + 12.0	I_q + 13.5	mA
$I_{R_DSI_2}$		DSI high [1]	$I_{R_DSI_1}$ + 10.5	$I_{R_DSI_1}$ + 12.0	$I_{R_DSI_1}$ + 13.5	mA
I_{R_PSI5}		PSI5 normal [1]	I_q + 22.0	I_q + 26.0	I_q + 30.0	mA
$I_{R_PSI5_Low}$		PSI5 low [1]	I_q + 11.0	I_q + 13.0	I_q + 15.0	mA
t_{INRUSH_60}	In-rush current: maximum time at peak current (C_{VBUF} = 1 µF)	In-rush current = 60 mA [2]	—	—	75	µs
t_{INRUSH_30}		In-rush current = 30 mA (limited by Master) [2]	—	—	200	µs
V_{BUF}	Internally regulated voltage (V_{BUF}, V_{BUS_I} = 4 V, V_{BUS_I} = 20 V)	[1]	2.85	3.00	3.15	V
$V_{BUS_I_UV_F}$	Low voltage detection threshold	BUS_I falling [1]	3.85	3.95	4.00	V
$V_{BUF_UV_F}$		V_{BUF} falling [1]	2.64	2.74	2.84	V
C_{VBUF}	V_{BUF} external capacitor	Capacitance [2]	100	1000	2000	nF
ESR		ESR (including interconnect resistance) [2]	0	—	200	mΩ
V_{DELTA_THRESH}	DSI3 V_{LOW} detection threshold (Section 11.2.1.1 "Command receiver")	$V_{LOW_min} \le (V_{BUS_I} - V_{SS}) \le V_{HIGH_max}$ V_{LOW} detection threshold [1]	V_{HIGH} – 1.25	V_{HIGH} – 1.0	V_{HIGH} – 0.75	V
R_{SENSE}	DSI3 discovery mode current sense (Section 11.2.2.3 "DSI3 discovery mode: address assignment method for resistor connected daisy chain devices")	Sense resistor [2]	1.0	1.3	3.0	W
I_{RESP_Offset}		I_{RESP} detection threshold ($I_{BUS_O_q} \le 24$ mA) [1]	6	12	18	mA
ΔV_{SYNC}	PSI5 synchronization pulse	$V_{PSI5_min} \le (V_{BUS_I} - V_{SS}) \le BUS_I_{MAX}$ DC sync pulse detection threshold [1]	V_{PSI5} + 1.0	V_{PSI5} + 1.5	V_{PSI5} + 2.0	V
I_{SYNC_PD}	PSI5 sync pulse pulldown current	[2]	—	I_{RESP_PSI5}	—	mA
$V_{BUSSW_L_OH}$	Bus switch output high voltage	BUSSW_L/INT, I_{Load} = –100 µA [1]	V_{BUF} – 0.35	—	V_{BUF}	V
$V_{BUSSW_L_OL}$	Bus switch output low voltage	BUSSW_L/INT, I_{Load} = 100 µA [1]	—	—	0.1	V
$I_{BUSSW_H_OL}$	Bus switch open-drain output current	V_{BUSSW_H} = V_{BUS_I} [1]	—	—	10	µA
$V_{BUSSW_H_OL}$	Bus switch output low voltage	BUSSW_H, I_{Load} = 100 µA [1]	—	—	0.1	V
Temperature sensor signal chain						
T_{RANGE}	Temperature measurement range	[2]	–50	—	+160	°C
T_{25}	Temperature output at 29 °C	[3]	83	93	103	LSB
T_{RANGE}	Range of output (8-bit)	Unsigned temperature [2]	0	—	255	LSB
T_{SENSE}	Temperature output sensitivity (8-bit)	[3]		1.00		LSB/°C
T_{ACC}	Temperature output accuracy (8-bit)	[4]	–10		+10	°C
T_{RMS}	Temperature output noise RMS (8-bit)	Standard deviation of 50 readings f_{Samp} = 8 kHz [1]	—	—	+2	LSB
Absolute pressure sensor signal chain						
P_{ABS}	Absolute pressure range	Maximum operating range [1]	40.00	—	132.8	kPa
P_0		Rated operating range: range at which ΔP/P_0 is valid [2]	47.30	—	115.2	kPa
P_{SENS}	Absolute pressure output sensitivity	P_CAL_ZERO = 0h 12-bit @ 0 Hz, tested @ P_{ABS}=100 kPa ± 10 % and 110 kPa ± 10 % [1]	—	28.75	—	LSB/kPa
P_{ACC_LoT1}	Absolute pressure accuracy	V_{CC} = 5.0 V –40 °C ≤ T_A < –20 °C [1] [5]	–2.0	—	+2.0	kPa
P_{ACC_LoT2}	Absolute pressure accuracy	V_{CC} = 5.0 V –20 °C ≤ T_A < 0 °C [1] [5]	–1.75	—	+1.75	kPa
P_{ACC_Typ}	Absolute pressure accuracy	V_{CC} = 5.0 V 0 °C ≤ T_A ≤ 85 °C [1] [5]	–1.25	—	+1.25	kPa
P_{ACC_HiT}	Absolute pressure accuracy	V_{CC} = 5.0 V 85 °C < T_A ≤ 125 °C [1] [5]	–2.0		+2.0	kPa

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Table 130. Static characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{OFF_D12}	Absolute pressure output @ 100 kPa	P_CAL_ZERO = 0h 12-bit [3]	—	2875	—	LSB
P_{OFF_D16}		P_CAL_ZERO = 0h 16-bit SNSDATAx register value [2]	—	34422	—	LSB
$PABS_{DNL}$	Absolute pressure nonlinearity	Absolute pressure DNL, 12-bit (monotonic with no missing codes) [3]	—	—	+1	LSB
$PABS_{INL}$		Absolute pressure INL, 12-bit (least squares BFSL) [3]	—	—	+20	LSB
$PABS_{RMS}$	Absolute pressure noise RMS (12-bit)	Standard deviation of 50 readings, f_{Samp} = 8 kHz, LPF = 370 Hz, 2-Pole, ambient pressure [3]	—	—	+2	LSB
$PABS_{Peak}$	Absolute pressure noise peak (12-bit)	Max. Deviation from Mean, 50 readings, f_{Samp} = 8 kHz, LPF = 370 Hz, 2-Pole, ambient pressure [3]	–8	—	+8	LSB
PSC_{PSI5}	Absolute pressure digital power supply coupling	C_{BUF} = 1 µf, 12-bit, DSI3, PSI5 1 kHz ≤ f_n ≤ 10 kHz, BUS_I = 8.0 V ± 2.0 V (represents PSI5 sync pulse) [2]	—	—	1	LSB
PSC_{DSI3R}		C_{BUF} = 1 µf, 12-bit, DSI3, PSI5 100 kHz ≤ f_n ≤ 1 MHz, BUS_I = 6.0 V ± 500 mV (represents DSI3/PSI5 response) [2]	—	—	1	LSB
PSC_{SATH}		C_{BUF} = 1 µf, 12-bit, DSI3, PSI5 1 MHz ≤ f_n ≤ 100 MHz, BUS_I = 6.0 V ± 50 mV (represents response harmonics) [2]	—	—	1	LSB
P_{ABS_RANGE}	Absolute pressure output range	Digital, 12-bit, typical full scale specified range [2]	1150	—	3818	LSB
P_{ABS_DErr}		Digital error response [6]	—	0	—	LSB
P_g	Sensitivity to Z-axis acceleration	Tested @ ±2000 g, t > 0.1 ms [2]	—	—	3.5	Pa/g
$P_{P\text{-}cell_Clip}$	Absolute pressure range, transducer	[6]	0	—	280	kPa
P_{ADC_Clip}	Absolute Pressure ΣΔ and Sinc filter clipping limit	[6]	0	—	280	kPa
Relative pressure sensor signal chain[7]						
P_{SENS}	Relative pressure sensitivity	P_CAL_ZERO = 0h 10-bit (± 5 %) [6]	28.5	30.00	31.5	LSB/%
$PREL_{DNL}$	Relative pressure nonlinearity	relative pressure differential nonlinearity, 10-bit (no missing codes) [6]	—	—	+1.0	LSB
$PREL_{INL}$		relative pressure integral nonlinearity, 10-bit (least squares BFSL) [2]	—	—	+20.0	LSB
DP_{OFF_D}	Relative pressure offset for constant pressure	$\Delta P/P_0$ = 0, P_CAL_ZERO = 0h 10-bit mean value of 50 readings, f_{Samp} = 8 kHz, DSI [2]	183	184	185	LSB
DP_{OFF_P}		$\Delta P/P_0$ = 0, P_CAL_ZERO = 0h 10-bit mean value of 50 readings, f_{Samp} = 8 kHz, PSI5 [2]	–329	–328	–327	LSB
DP_{OFF_16}		$\Delta P/P_0$ = 0,P_CAL_ZERO = 0h 16-bit SNSDATAx register value, mean value of 50 readings, f_{Samp} = 8 kHz [2]	—	30144	—	LSB
$PREL_{RMS}$	Relative pressure RMS noise	$\Delta P/P_0$ = 0, 10-bit Standard deviation of 50 readings, f_{Samp} = 8 kHz [2]	—	—	1	LSB
$PREL_{Peak}$	Relative pressure noise peak	$\Delta P/P_0$ = 0, 10-bit Max. deviation from mean, 50 readings, f_{Samp} = 8 kHz [2]	–4	—	+4	LSB
DP	Relative pressure output full-scale range	DSI3, PSI5, 10-bit, PREL guaranteed from –5 % to +26.9 % [6]	1	—	1023	LSB
DP_{ERR}		DSI3 error response [2]	—	0	—	LSB
DP		PSI5 data with DATA_EXT = 0 [2] [8]	–102	—	+307	LSB
DP		PSI5 data with DATA_EXT = 1 [2] [8]	–480	—	+480	LSB

[1] Parameter verified by final test.
[2] Parameter verified by functional evaluation.
[3] Functionality verified by characterization.
[4] Parameter verified by qualification.
[5] See Section 6.7 for accuracy over temperature and life, including nonlinearity, full scale = PABS range.
[6] Functionality verified by modeling, simulation and/or design verification.

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[7] The Relative pressure sensor signal chain section of this table refers to DATA_EXT = 0
[8] See Table 156, PSI5 data values for DATA_EXT = 0 and DATA_EXT = 1.

10 Dynamic characteristics

$V_{BUS_I_L_min} \le (V_{BUS_I} - V_{SS}) \le V_{BUS_I_H_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Table 131. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DSI3						
t_{VHIGH_RC}	Command reception (general)	V_{HIGH} low-pass filter time constant (Section 11.2.1.1 "Command receiver") [1]	60	120	180	µs
t_{VHIGH_Delay}		V_{HIGH} detection analog delay (Section 11.2.1.1 "Command receiver") [1]	—	—	600	µs
t_{Cmd_Valid}		Command valid time (Section 11.2.1.1 "Command receiver") [1]	—	2	—	µs
t_{SLEW1_RESP}	Response transmission (general, slew control enabled, Section 11.2.3.3 "DSI3 command and response mode timing")	Response slew time: 2.0 mA to 10.0 mA, 10.0 mA to 2.0 mA [1]	350	400	500	ns
t_{SLEW2_RESP}		Response slew time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA [1]	350	400	500	ns
Δt_{SLEW}		$t_{SLEW1_RESP} - t_{SLEW2_RESP}$ [1]	–100	—	100	ns
Δt_{SLEW_rf}		$t_{SLEW1_RESP_Rise} - t_{SLEW2_RESP_Fall}$ [1]	–250	—	250	ns
t_{ACT_RESP}		Response current activation time: current activated to 50 % [1]	200	—	400	ns
t_{nSLEW1_RESP}	Response transmission (general, slew control disabled, Section 11.2.3.3 "DSI3 command and response mode timing")	Response slew time: 2.0 mA to 10.0 mA, 10.0 mA to 2.0 mA [1]	—	—	300	ns
t_{nSLEW2_RESP}		Response slew time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA [1]	—	—	300	ns
Δt_{nSLEW}		$t_{SLEW1_RESP} - t_{SLEW2_RESP}$ [1]	–300	—	300	ns
Δt_{nSLEW_rf}		$t_{SLEW1_RESP_Rise} - t_{SLEW2_RESP_Fall}$ [1]	–300	—	300	ns
t_{nACT_RESP}		Response current activation time: Current activated to 50 % [1]	—	—	300	ns
t_{START_DISC}	Command reception (discovery mode)	Command start time (Section 11.2.2 "Address assignment") [1]	t_{POR_DSI}	—	13.5	ms
$t_{DISC_BitTime}$		Command bit time (Section 11.2.2 "Address assignment") [1]	14	16	18	µs
t_{PER_DISC}		Command transmission period (Section 11.2.2 "Address assignment") [1]	125	—	—	µs
$t_{CmdBlock_DISC}$		Command blocking time, discovery mode (Section 11.2.1.1 "Command receiver") [1]	—	96	—	µs
t_{DISC_DLY}	Response transmission (discovery mode)	Idle current sample delay (Section 11.2.2 "Address assignment") [1]	—	48	—	µs
$t_{DISC_ICCQ_SAMP}$		Idle current sample time (Section 11.2.2 "Address assignment") [1]	—	15	—	µs
$t_{START_DISC_RSP}$		Response start delay (Section 11.2.2 "Address assignment") [1]	—	64	—	µs
$t_{DISC_Ramp_RSP}$		Response ramp time (Section 11.2.2 "Address assignment") [1]	—	16	—	µs
I_{DISC_Ramp}		Response ramp rate (Section 11.2.2 "Address assignment") [1]	—	1.5	—	mA/µs
$t_{DISC_Idle_RSP}$		Response idle time (Section 11.2.2 "Address assignment") [1]	—	16	—	µs
I_{DISC_Peak}		Response peak current (Section 11.2.2 "Address assignment") [1]	—	$2*I_{RESP}$	—	mA
$t_{IDISC_Samp_Dly}$		Response current sample delay (Section 11.2.2 "Address assignment") [1]	—	65	—	µs
t_{IDISC_Samp}		Response current sample time (Section 11.2.2 "Address assignment") [1]	—	31	—	µs

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Table 131. Dynamic characteristics*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{Cmd_BitTime}$	Command reception (command and response mode)	Command bit time (Section 11.2.3 "DSI3 command and response mode") [1]	—	8	—	µs
t_{PER_CRM}		Command transmission period (Section 11.2.3 "DSI3 command and response mode") [1]	475	—	—	µs
$t_{CmdBlock_CRM}$		Command blocking time, CRM (Section 11.2.1.1 "Command receiver") [1]	—	455	—	µs
$t_{CmdBlock_ST_CRM}$		Command blocking start time, CRM (Section 11.2.1.1 "Command receiver") [1]	—	290	—	µs
t_{CHIP_CRM}	Response transmission (command and response mode)	Response chip time [1]	—	5	—	µs
t_{START_CRM}		Response start time (Section 11.2.3 "DSI3 command and response mode") [1]	—	295	—	µs
$t_{Cmd_BitTime}$	Command reception (periodic data collection mode)	Command bit time (Section 11.2.4 "DSI3 periodic data collection mode and background diagnostic mode") [1]	—	8	—	µs
t_{PER_PDCM}		Command transmission period (Section 11.2.4 "DSI3 periodic data collection mode and background diagnostic mode") [1]	100	—	—	µs
t_{CHIP_PDCM}	Response transmission (periodic data collection mode)	Response chip time typical (Section 6.2.14 "CHIPTIME – chip time and bit time register (address $23)") [1]	1.0	—	5.0	µs
$t_{START_PDCM_Min}$		Min programmed start time: PDCM_RSPSTx < 0015h [1]	—	20	—	µs
$t_{START_PDCMBDMMin}$		Min programmed start time: BDM enabled [1]	—	51	—	µs
$t_{START_PDCM_Max}$		Max programmed start time: PDCM_RSPSTx = 1FFFh [1]	—	8191	—	µs
t_{CHIP_CRM}	Response transmission (Background Diagnostic mode)	Response chip time [1]	—	5	—	µs
t_{START_BDM}		Response start time (Section 11.2.4 "DSI3 periodic data collection mode and background diagnostic mode") [1]	—	20	—	µs
t_{LAT_DSI}	DSI data latency	[2]	0	—	2.00	µs
$t_{OTP_WRITE_MAX}$	OTP program timing	Time to program an OTP user region [1]	—	—	10	ms
PSI5						
t_{PSI5_INIT1}	Initialization timing	Phase 1 [1]	—	133	—	ms
$t_{PSI5_INIT2_10s}$		Phase 2 (10-bit, synchronous mode, k = 4, t_{S-S} = 500 µs) [1]	—	256 * t_{S-S}	—	s
$t_{PSI5_INIT2_10a}$		Phase 2 (10-bit, asynchronous mode, k = 8) [1]	—	512 * t_{ASYNC}	—	s
$t_{PSI5_INIT3_10s}$		Phase 3 (10-bit, synchronous mode, t_{S-S} = 500 µs) [1]	—	6 * t_{S-S}	—	s
$t_{PSI5_INIT3_10a}$		Phase 3 (10-bit, asynchronous mode) [1]	—	6 * t_{ASYNC}	—	s
t_{PSI5ST_START}		PSI5 self-test start time [1]	—	50	—	ms
t_{ST_INIT}		PSI5 self-test time [1]	—	64	—	ms
t_{ST_P0INIT}		PSI5 post self-test P0 initialization time [1]	—	128	—	ms
ST_RPT		Self-test repetitions [1]	0	—	8	
t_{PME}		Programming mode entry window [1]	—	127	—	ms

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Table 131. Dynamic characteristics*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RS_PM}	Synchronization pulse	Reset to first sync pulse (Program mode entry) [1]	6	—	—	ms
t_{RS}		Reset to first sync pulse (Normal mode) [1]	t_{PSI5_INIT1}	—	—	s
t_{S-S}		Sync pulse period [1]	175	—	—	µs
t_{SYNC}		Sync pulse width [1]	9	—	—	µs
t_{SYNC_LPF}		Sync pulse reference LPF time constant [1]	120	280	—	µs
$t_{SYNC_LPF_RST_ST}$		Sync pulse reference discharge start time [1]	—	9.0	—	µs
$t_{SYNC_LPF_RST}$		Sync pulse reference discharge activation time [1]	—	154	—	µs
$t_{SYNC_OFF_500}$		Sync pulse detection disable time (PDCM_CMD_B = 0) [1]	—	450	—	µs
$t_{SYNC_OFF_250}$		PME sync pulse detection disable time [1]	—	225	—	µs
$t_{A_SYNC_DLY}$		Analog delay of sync pulse detection [1]	50	—	600	µs
t_{PD_DLY}		Sync pulse pulldown function delay time [1]	—	9.0	—	µs
t_{PD_ON}		Sync pulse pulldown function activates time [1]	—	16	—	µs
t_{SYNC_JIT}		Sync pulse detection jitter [1]	0	—	0.5	µs
$t_{BIT_Standard}$	Data transmission single bit time	PSI5 standard bit rate [1]	—	8.00	—	µs
t_{BIT_HI}		PSI5 high bit rate [1]	—	5.30	—	µs
t_{SLEW1_RESP}	Response current transmission	No external components Response slew time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA [1]	350	400	500	ns
$t_{Bittrans_LowBaud}$	Position of bit transition	All except 5.3 µs [1]	49	50	51	%
$t_{Bittrans_HighBaud}$		5.3 µs [1]	49	—	51	%
t_{ASYNC}	Asynchronous response time	[1]	—	228	—	µs
$t_{TIMESLOTx_MIN}$	Time slots	Min programmed time slot: PDCM_RSPSTx < 0014h [1]	—	20	—	µs
$t_{TIMESLOTx_MAX}$		Max programmed time slot: PDCM_RSPSTx = 1FFFh [1]	—	8191	—	µs
$t_{TIMESLOT_DFLT}$		Default time slot (PDCM_RSPSTx = 0000h) [1]	—	20	—	µs
$t_{TIMESLOTx_RES}$		Time slot resolution [1]	—	1.0	—	µs/LSB
$t_{TIMESLOT_DC0}$		Sync pulse to daisy chain default time slot 0 [1]	—	46.5	—	µs
$t_{TIMESLOT_DC1_L}$		Sync pulse to daisy chain default time slot 1 (low) [1]	—	192	—	µs
$t_{TIMESLOT_DC2_L}$		Sync pulse to daisy chain default time slot 2 (low) [1]	—	350	—	µs
$t_{TIMESLOT_DC1_H}$		Sync pulse to daisy chain default time slot 1 (high) [1]	—	150	—	µs
$t_{TIMESLOT_DC2_H}$		Sync pulse to daisy chain default time slot 2 (high) [1]	—	260	—	µs
$t_{TIMESLOT_DC3_H}$		Sync pulse to daisy chain default time slot 3 (high) [1]	—	380	—	µs
$t_{TIMESLOT_DCP}$		Sync pulse to daisy chain programming time slot [1]	—	46.5	—	µs
t_{LAT_PSI5}	PSI5 data latency	[2]	0	—	1.00	µs
t_{BUS_SW}	Bus switch output activation time	C = 50 pF From last bit of SetAdr response to 80 % of $V_{BUS_SW_OH}$ [1]	—	—	300	µs
t_{S-S_PM}	Diagnostic and programming mode sync pulse period	The user must provide a sync pulse period within this range to guarantee DPM communications [1]	245	250	255	µs
t_{S-S_DC}	Daisy chain mode sync pulse period	The user must provide a sync pulse period within this range to guarantee communications [1]	490	500	510	µs
$t_{OTP_WRITE_MAX}$	OTP program timing	Time to program one OTP user region [1]	—	—	10	ms

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Table 131. Dynamic characteristics*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Signal chain						
$t_{SigChain}$	Signal chain sample time	[2]	—	48	—	µs
f_{c0}	P_{ABS} low-pass filter cut-off frequency	Filter option #0, 2-pole [1]	—	370	—	Hz
f_{c1}		Filter option #1, 3-pole [1]	—	400	—	Hz
f_{c2}		Filter option #2, 4-pole [1]	—	800	—	Hz
f_{c3}		Filter option #3, 4-pole [1]	—	1000	—	Hz
$t_{0CSAMP0}$ (Design data available)	P_0 low-pass filter sample time	Phase 0 [1]	—	384	—	µs
f_{OC0}	P_0 low-pass filter cut-off frequency	Phase 0, 1-pole [1] [2]	—	163.8	—	Hz
t_{OC0}	P_0 low-pass filter time in phase	Phase 0 [1] [2]	—	4.096	—	ms
$t_{0CSAMP1}$	P_0 low-pass filter sample time	Phase 1 [1] [2]	—	384	—	µs
f_{OC1}	P_0 low-pass filter cut-off frequency	Phase 1, 1-pole [1] [2]	—	40.96	—	Hz
t_{OC1}	P_0 low-pass filter time in phase	Phase 1 [1] [2]	—	4.096	—	ms
$t_{0CSAMP2}$	P_0 low-pass filter sample time	Phase 2 [1] [2]	—	384	—	µs
f_{OC2}	P_0 low-pass filter cut-off frequency	Phase 2, 1-pole [1] [2]	—	10.24	—	Hz
t_{OC2}	P_0 low-pass filter time in phase	Phase 2 [1] [2]	—	16.388	—	ms
$t_{0CSAMP3}$	P_0 low-pass filter sample time	Phase 3 [1] [2]	—	384	—	µs
f_{OC3}	P_0 low-pass filter cut-off frequency	Phase 3, 1-pole [1] [2]	—	2.560	—	Hz
t_{OC3}	P_0 low-pass filter time in phase	Phase 3 [1] [2]	—	65.53	—	ms
$t_{0CSAMP4}$	P_0 low-pass filter sample time	Phase 4 [1] [2]	—	384	—	µs
f_{OC4}	P_0 low-pass filter cut-off frequency	Phase 4, 1-pole [1] [2]	—	0.6400	—	Hz
t_{OC4}	P_0 low-pass filter time in phase	Phase 4 [1] [2]	—	262.19	—	ms
$t_{0CSAMP5}$	P_0 low-pass filter sample time	Phase 5 [1] [2]	—	384	—	µs
f_{OC5}	P_0 low-pass filter cut-off frequency	Phase 5, 1-pole [1] [2]	—	0.1600	—	Hz
t_{OC5}	P_0 low-pass filter time in phase	Phase 5 [1] [2]	—	1049	—	ms
$t_{0CSAMP6}$	P_0 low-pass filter sample time	Phase 6 [1] [2]	—	384	—	µs
f_{OC6}	P_0 low-pass filter cut-off frequency	Phase 6, 1-pole [1] [2]	—	0.1600	—	Hz
t_{RD_Rate}	P0 global filter gradient (Section 6.6.4.4 "P0 low-pass filter and gradient filter") (typical = 400 Pa/s) Rate limiting output update time	[1] [2]	—	0.025	—	s
OFF_{Step}	P0 global filter gradient (Section 6.6.4.4 "P0 low-pass filter and gradient filter") (typical = 400 Pa/s) Rate limiting output step size (12-bit)	[1] [2]	—	0.5	—	LSB
$t_{SigDelay}$(Design data only)	Signal delay	Sinc filter to output delay, excluding the P_{ABS} and P_0 LPF [1] [2]	—	—	128	µs
t_{INTERP}	Interpolation	[1] [2]	—	3	—	µs
t_{LAT_INTERP} (GBD)	Interpolation latency	[1] [2]	—	$t_{SigChain}$	—	µs
t_{ST_INIT}	P_{ABS} startup common mode verification test time	[1] [2]	—	65	70	ms
$t_{ST_Resp_1000_4}$	Self-test response time	Digital self-test activation/deactivation to final value LPF = 1000 Hz, 4-pole [1] [2]	—	12	15	ms
$t_{ST_Resp_370_3}$	Self-test response time: digital self-test	Digital self-test activation/deactivation to final value LPF = 370 Hz, 2-pole [1] [2]	—	25	30	ms
$t_{ST_FP_Resp}$	Fixed pattern response time	Self-test activation/deactivation [1]	—	—	100	µs
f_{PCELL}	Sensing element resonant frequency	[2]	—	—	—	kHz
$f_{Package}$	Package resonance frequency	[2]	100	—	—	kHz

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Table 131. Dynamic characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply and support circuitry						
t_{VCC_POR}	Reset recovery	All modes, excluding V_{BUS_I} voltage ramp time VCC = VCCMIN to POR release [1]	—	—	1	ms
t_{POR_DSI}		All modes, excluding V_{BUS_I} voltage ramp time POR to 1st DSI command (Section 11.2.1 "DSI3 physical layer") [1]	—	—	6	ms
t_{POR_PSI5}		All modes, excluding V_{BUS_I} voltage ramp time POR to PSI5 initialization phase 1 start (Section 11.3.4 "Initialization") [1]	—	—	6	ms
$t_{POR_DataValid}$		All modes, excluding V_{BUS_I} voltage ramp time POR to sensor data valid [1]	—	—	30	ms
$t_{RANGE_DataValid}$		All modes, excluding V_{BUS_I} voltage ramp time DSP setting change to sensor data valid [1]	—	—	6	ms
$t_{SOFT_RESET_DSI}$	Soft reset activation time	DSI3: command/response complete to reset [1]	—	—	11	µs
$t_{SOFT_RESET_PSI}$		PSI5: command/response complete to reset [1]	—	—	50	µs
fOSC	Internal oscillator period	Untrained [1] [2]	9.500	10.000	10.500	MHz
f_{OSC_TRAIN}		With oscillator training [1] [2]	9.900	10.000	10.100	MHz
t_{OSC_TRAIN}	Oscillator training (Section 6.5.1 "Oscillator training")	Oscillator training time [1] [2]	—	4	—	ms
nOSC_4ms_TYP		Oscillator cycles in training time [1] [2]	—	40000	—	$1/f_{OSC}$
OscTrainWIN		Oscillator training window [1] [2]	38000	—	42000	$1/f_{OSC}$
OscTrainADJ		Oscillator training adjustment threshold [1] [2]	–400	—	400	$1/f_{OSC}$
OscTrainRES		Oscillator training step size [1] [2]		250		$1/f_{OSC}$
t_{SET}	Quiescent current settling time	Power applied to Iq = I_{IDLE} +/- 2 mA [1]	—	—	4	ms
$t_{BUS_I_MICROCUT}$	BUS_I micro-cut survival time	BUS_I disconnect without reset, C_{BUF} = 1 µF, bus with 1 slave [1]	30	—	—	ms
$t_{BUS_I_RESET}$	BUS_I micro-cut reset time	BUS_I disconnect time to reset, C_{BUF} = 1 µF, bus with 1 slave [1]	—	—	1000	ms
$t_{BUS_I_MICROCUT}$	BUS_I micro-cut survival time	BUS_I disconnect without reset, C_{BUF} = 100 nF, Bus with 1 slave [1]	0.5	—	—	ms
$t_{BUS_I_RESET}$	BUS_I micro-cut reset time	BUS_I disconnect time to reset, C_{BUF} = 100 nF, bus with 1 slave [1]	—	—	1000	ms
$t_{BUS_I_MICROCUT}$	BUS_I micro-cut survival time	BUS_I disconnect without reset, C_{BUF} = 0 nF, bus with 1 slave [1]	0	—	—	ms
$t_{BUS_I_RESET}$	BUS_I micro-cut reset time	BUS_I disconnect time to reset, C_{BUF} = 0 nF, bus with 1 slave [1]	—	—	1000	ms
$t_{BUS_I_POR}$	BUS_I undervoltage detection delay	BUS_I < $V_{BUS_I_UV_F}$ to I_{RESP} deactivation [1]	—	—	5	µs
t_{VBUF_POR}	V_{BUF} undervoltage detection delay	V_{BUF} < $V_{BUF_UV_F}$ to I_{RESP} deactivation [2]	—	—	5	µs
t_{UVOV_RCV}	Undervoltage/overvoltage recovery delay	[2]	—	100	—	µs
$t_{D_CAPTEST}$	V_{BUF} capacitor monitor	DSI command start to capacitor test [2]	—	4.0	—	µs
$t_{P_CAPTEST}$	V_{BUF} capacitor monitor	PSI5 synchronous command start to capacitor test [2]	—	9.2	—	µs
$t_{A_CAPTEST}$	V_{BUF} capacitor monitor	PSI5 asynchronous response start to capacitor test [2]	—	179.2	—	µs
t_{CAPTST_TIME} (validation only)	V_{BUF} capacitor monitor	Capacitor test disconnect time [2]	—	1	—	µs

[1] Parameter verified by functional evaluation.
[2] Functionality verified by modeling, simulation and/or design verification.

11 Application information

Note: *A gel is used to provide media protection against corrosive elements which may otherwise damage metal bond wires and/or IC surfaces. Highly pressurized gas molecules may permeate through the gel and*

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occupy boundaries between material surfaces within the sensor package. When decompression occurs, the gas molecules may collect, form bubbles and possibly result in delamination of the gel from the material it protects. If a bubble is located on the pressure transducer surface, or on the bond wires, the sensor measurement may shift from its calibrated transfer function. In some cases, these temporary shifts could be outside the tolerances listed in the data sheet. In rare cases, the bubble may bend the bond wires and result in a permanent shift.

11.1 Media compatibility – pressure sensors only

For more information regarding media compatibility, contact your local sales representative.

Note:

The devices contain a gel that protects the pressure transducer and its inter-die connection wires from corrosion, which might otherwise result in catastrophic failure modes. NXP has observed that direct exposure to materials with the same or nearly-the-same solubility can potentially result in a corruption of the protective gel. A corruption can be less than catastrophic in nature, however may result in an offset of the pressure measurement from its factory calibrated value. An offset can potentially be larger than the allowed tolerances published in this data sheet.

Further, NXP does not recommend direct exposure to strong acid or strong base compounds as they can potentially result in a similar corruption as described above, or may result in a dissolution of the protective gel and/or the metal lid adhesive and/or the plastic device body. Such a dissolution can be catastrophic in nature, damaging the transducer surfaces and/or internal wire bonds and/or the control die surfaces. A potential dissolution may result in a similar offset, or cause the device to indicate overflow/underflow status, or may cause the device to cease operating in the worst case.

For a list of compounds known to generate out-of-tolerance offsets and/or catastrophic device failure, please contact an NXP sales representative.

11.2 DSI3 protocol

The DSI3 standard[1] describes two function classes: signal function class and power function class. The device is a slave conforming to the signal function class requirements. The device does not support power function class. This section describes the DSI3 signal function class features supported by the device.

11.2.1 DSI3 physical layer

11.2.1.1 Command receiver

The command receive block converts voltage transitions on the BUS_I pin to a digital pulse train for decoding by the DSI data link layer.

The supply voltage can vary throughout the specified range, so the communication high voltage (V_{HIGH}) must be sampled and averaged with a low-pass filter. The communication low voltage is then determined by comparing the supply voltage to the sampled and averaged V_{HIGH} voltage. Figure 27 shows a block diagram of the command receiver physical layer.

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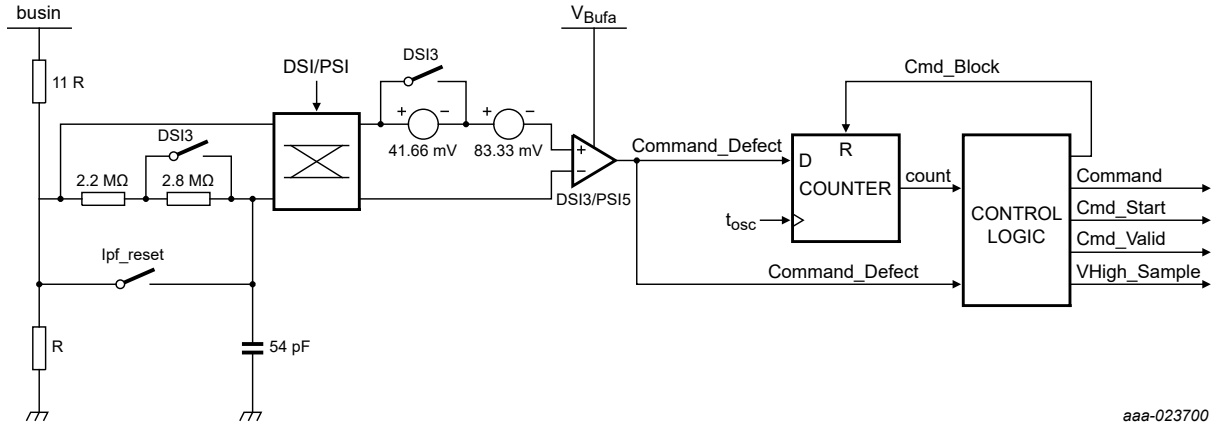


Figure 27. Command receiver physical layer

The start of a command is detected when the comparator output (Command_Detect) is low. The comparator output is input to a counter that is updated at the internal oscillator frequency. Control logic monitors the counter output and generates the necessary internal signals for the logic.

Figure 28 shows a timing diagram of the command receiver when a valid command is received, and Figure 29 shows a timing diagram of the command receiver when a microcut is received during the command window. Voltage values and timing parameters are specified in Section 9 "Static characteristics" and Section 10 "Dynamic characteristics".

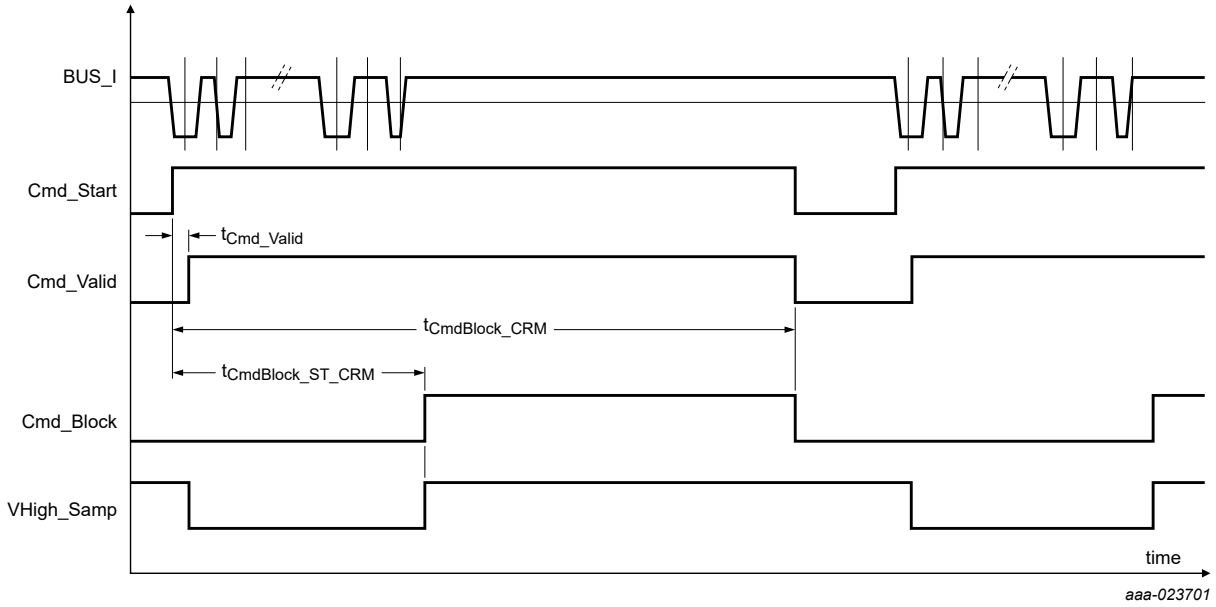


Figure 28. DSI3 command receiver timing diagram: valid command

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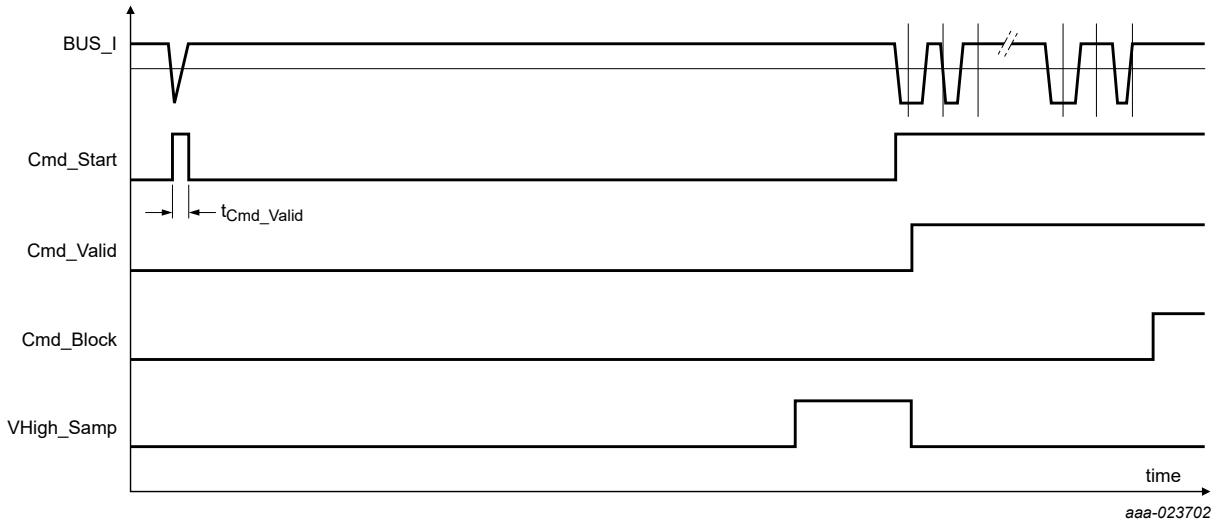


Figure 29. DSI3 command receiver timing diagram: microcut

11.2.1.2 Response transmitter

The response transmitter block converts two digital signals into two supply modulation current. The response currents are generated such that the rise and fall times are the same whether the I_{RESP} current is being transmitted or the 2 x I_{RESP} current is being transmitted. A diagram of the response transmitter is shown in Section 11.2.1.1 "Command receiver". Current values and timing parameters are specified in Section 9 "Static characteristics" and Section 10 "Dynamic characteristics".

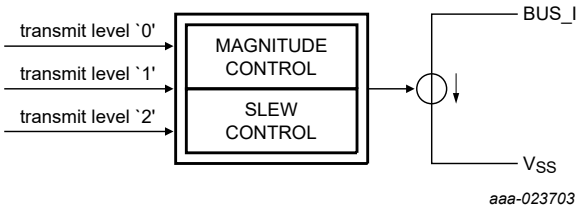


Figure 30. DSI3 transmitter block diagram

11.2.1.3 Discovery mode current sense

The current sense circuit is used during discovery mode to determine if any additional slaves are connected to the BUS_O pin of the device. A diagram of the current sense circuit is shown in Figure 31. Current values and timing parameters are specified in Section 9 "Static characteristics" and Section 10 "Dynamic characteristics". Details regarding discovery mode are included in Section 11.2.2.3 "DSI3 discovery mode: address assignment method for resistor connected daisy chain devices".

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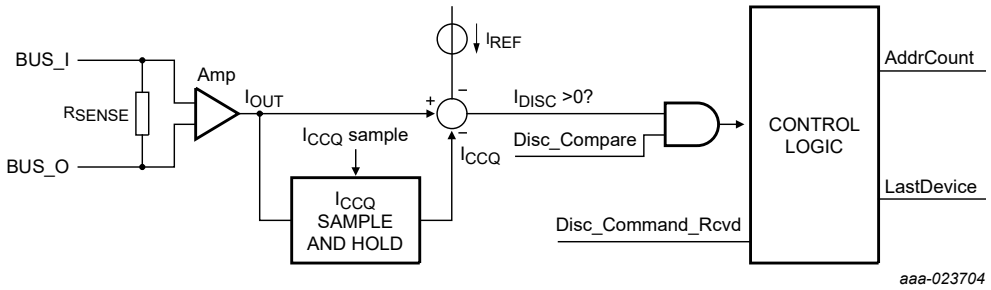


Figure 31. Discovery mode current sense circuit block diagram

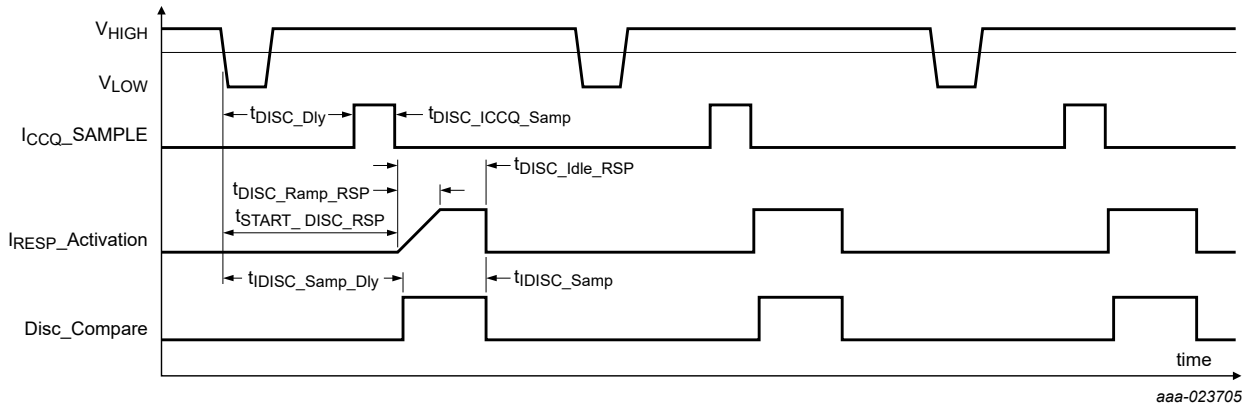


Figure 32. DSI3 discovery mode sensing timing diagram

11.2.2 Address assignment

The device supports all three address assignment methods and described in the DSI3 standard[1] and in the following sections.

11.2.2.1 Address assignment method for parallel connected slaves

Devices connected in parallel must have preprogrammed addresses by storing a nonzero value into the PADDR[3:0] bits of the PHYSADDR OTP register. If a nonzero value is stored in this OTP register, the device does not participate in any other address assignment method and waits for command and response mode for further configuration. See Section 11.2.3 "DSI3 command and response mode" for details regarding command and response mode.

11.2.2.2 Address assignment method for bus switch connected daisy chain devices

A device connected in daisy chain by a bus switch may have either a preprogrammed address as described in Section 11.2.2.1 "Address assignment method for parallel connected slaves", or an unprogrammed address.

If the address is preprogrammed, the device does not participate in any other address assignment method and waits for command and response mode for further configuration information, including activating the bus switch to connect the next device on the bus. See Section 11.2.3 "DSI3 command and response mode" for details regarding command and response mode.

If the address is unprogrammed, once power is applied, the device is the only device on the segment that requires an address assignment. The device will accept a command and response mode register write command addressed to Address $0 (global command), which writes the PADDR[3:0] bits to a nonzero value.

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Once a physical address is assigned to the device, command and response mode is used with the assigned physical address for further configuration.

On power up, the device bus switch output defaults to deactivated.

11.2.2.3 DSI3 discovery mode: address assignment method for resistor connected daisy chain devices

A device connected in daisy chain via a resistor has an unprogrammed address and uses discovery mode to obtain its physical address (PADDR[3:0]).

The master device must initiate discovery mode automatically after power is applied to the bus segment by sending a sequence of discovery commands. Discovery mode timing is defined in Section 10 "Dynamic characteristics". If the ENDINIT bit is not set and the PADDR[3:0] field is set to '0000', the device will detect a discovery command t_{START_DISC} after a power-on-reset and for intervals of t_{PER_Disc} until discovery mode has ended (the maximum value of t_{START_DISC}).

Figure 31 shows a timing diagram of the discovery protocol for a four-device segment. The discovery mode follows this sequence:

1. The master powers up the bus segment to a known state.
2. The master transmits the discovery command.
3. After a predetermined delay ($t_{START_DISC_RSP}$), all devices without a physical address activate a current ramp to the 2x response current at a ramp rate of i_{DISC_RAMP}.
4. Each device monitors the current through its sense resistor (Δi_{SENSE}).
   a. If the current is above i_{RESP}, the device disables its response current, increments its physical address counter, and waits for the next Discovery Command.
   b. If the current is low (Δi_{SENSE} less than i_{RESP}), the device continues to ramp its response current to 2 x i_{RESP} in time $t_{DISC_RAMP_RSP}$ and maintains the current at 2 x i_{RESP} for time $t_{DISC_IDLE_RSP}$.
   c. After time $t_{DISC_IDLE_RSP}$, if a device has not detected a current through its current sense resistor of i_{RESP}, the device accepts physical address '1' and disables its response current.
5. After a predefined period (t_{PER_DISC}), the master transmits another discovery command.
6. Steps 3 and 4 are repeated, with the device accepting the address in its address assignment counter if the sense current is low.
7. The master repeats step 5 until it has transmitted discovery commands for all the devices it expects on the bus.
8. Device initialization can now begin using command and response mode.

Once the discovery mode is complete, a physical address is assigned to the device, and command and response mode is used with the assigned physical address for further configuration.

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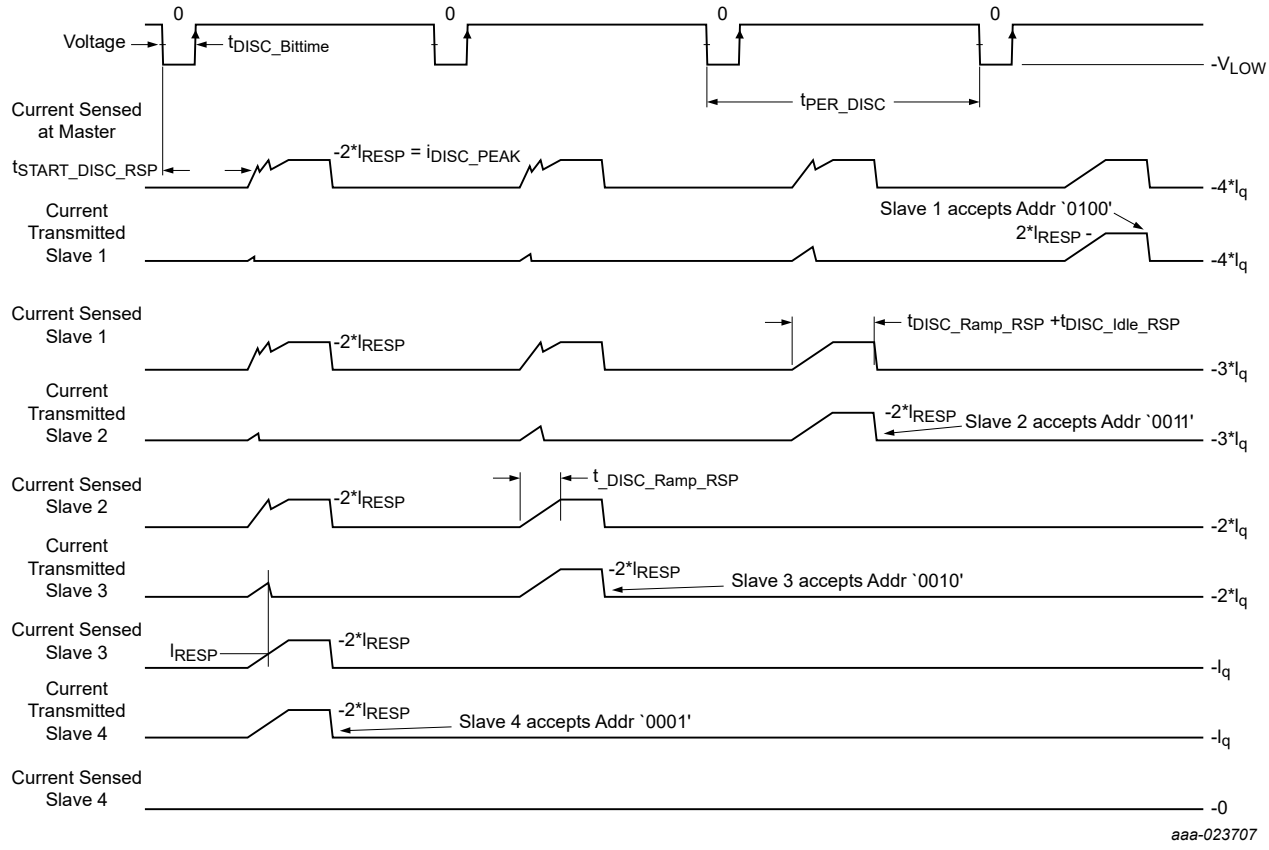


Figure 33. DSI3 discovery mode timing diagram

11.2.3 DSI3 command and response mode

DSI3 command and response mode is the main communication method used for initialization of the device.

11.2.3.1 DSI3 command and response mode command reception

Command and response mode data packets are exchanged between a single master and a single slave. The primary purpose of command and response transactions are to read from and write to registers within the device memory structure.

A command and response mode command example is shown in Figure 34. The command consists of 32 bits of data broken up into multiple fields as described in Section 11.2.3.1.2 "Command message format".

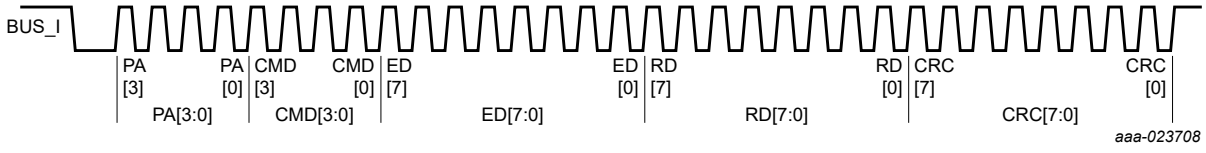


Figure 34. Command and response mode command example

Physical address				Command				Extended data								Register data								Error checking							
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E7	E6	E5	E4	E3	E2	E1	E0
0	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	1	0	1	1	0

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11.2.3.1.1 Bit encoding

Figure 35 shows the bit encoding used for command and response mode commands from the master device.

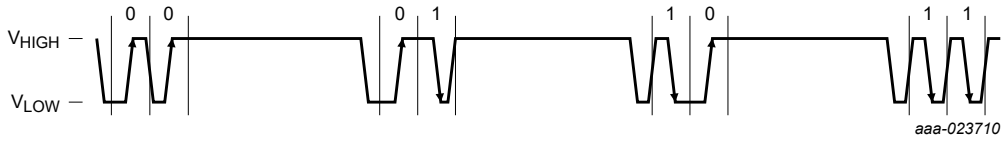


Figure 35. Command and response mode command bit encoding

11.2.3.1.2 Command message format

The command and response mode command format is shown in Table 132.

Table 132. Command and response mode – command format

Physical address	Command	Extended data	Register data	CRC
PA[3:0]	CMD[3:0]	ED[7:0]	RD[7:0]	CRC[7:0]

Table 133. Command and response mode – field definitions

Field	Length (bits)	Definition
PA[3:0]	4	Physical address Must match the value in the PADDR[3:0] of the PHYSADDR register
CMD[3:0]	4	Command (see Section 11.2.3.4 "DSI3 command and response mode command summary")
ED[7:0]	8	Extended data (see Section 11.2.3.4 "DSI3 command and response mode command summary")
RD[7:0]	8	Register data (see Section 11.2.3.4 "DSI3 command and response mode command summary")
CRC[7:0]	8	Error checking (see Section 11.2.3.1.3 "Error checking")

11.2.3.1.3 Error checking

The device calculates an 8-bit CRC on the entire 32 bits of each command. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message. If the calculated CRC does not match the transmitted CRC, the command is ignored and the device does not respond.

The CRC decoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial and seed for command and response mode are shown in Table 134.

Table 134. Command and response mode command CRC

Mode	Default polynomial	Nondirect seed
Command and response	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111

Some example CRC calculations are shown in Table 135.

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Table 135. Command and response mode – CRC calculation examples

Physical address	Command	Extended data	Register data	Nondirect seed	8-bit CRC
01h	08h	11h	86h	FFh	B0h
02h	01h	25h	FFh	FFh	38h
03h	0Fh	1Ah	41h	FFh	2Ch
04h	01h	01h	01h	FFh	D4h

11.2.3.2 DSI3 command and response mode response transmission

An example command and response mode response is shown in Figure 36. The response consists of 32 bits of data broken up into multiple fields as described in Section 11.2.3.2.2 "Response message format".

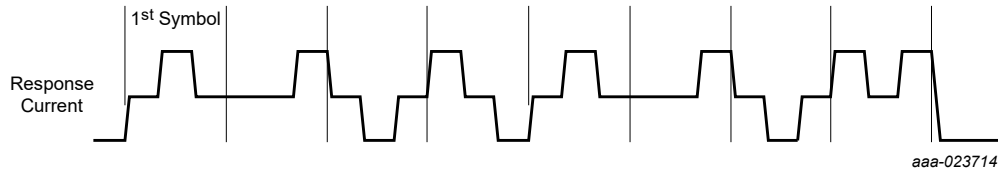


Figure 36. Command and response mode response example

Physical address				Command				Extended data								Register data								Error checking							
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E7	E6	E5	E4	E3	E2	E1	E0
0	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	0	0	0	1	1	0	1	1	0

11.2.3.2.1 Symbol encoding

The device response to a command and response mode command uses multilevel source coding where data nibbles are first encoded into symbols and then the symbols are encoded into current levels. The symbols are assembled from three consecutive three-level current pulses called chips. Within a symbol there are three consecutive chips that can assume one of three discrete current levels as described in Section 9 "Static characteristics": i_q, $i_q + i_{RESP}$, and iq + 2 x i_{RESP}. Figure 37 shows the chip transmissions and an example of a three symbol (nine chip), 12-bit data packet.

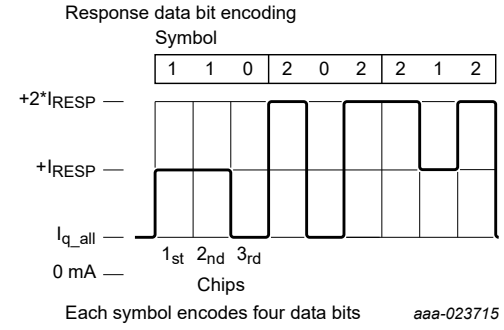


Figure 37. Response symbol encoding

Of the 27 possible combinations for three consecutive trilevel chips, the combinations that begin with the null current level (i_q) are discarded. Of the remaining 18 symbols, the two symbols that contain the same value for all three chips are also discarded. The remaining 16 symbols all begin with a non-null current level and have at least one transition. These characteristics guarantee that any response packet has a transition at the beginning of a packet and at least one transition in every symbol. Each three-chip symbol encodes the information of four bits. Table 136 shows the symbol encoding used by the device.

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Table 136. Symbol mapping

Encoded data (4 bits)		Symbol transmitted		
Binary	Hex	1st chip	2nd chip	3rd chip
0000	0	1	1	0
0001	1	2	1	1
0010	2	1	0	2
0011	3	2	0	2
0100	4	1	0	0
0101	5	2	1	2
0110	6	1	1	2
0111	7	2	0	1
1000	8	2	2	0
1001	9	2	1	0
1010	A	1	2	2
1011	B	2	2	1
1100	C	1	2	0
1101	D	2	0	0
1110	E	1	0	1
1111	F	1	2	1

Where:

0 = iq

1 = i_{RESP}

2 = 2 x i_{RESP}

11.2.3.2.2 Response message format

The command and response mode response format is shown in Table 137 .

Table 137. Command and response mode – response format

Physical address	Command	Register + 1 data	Register data	CRC
PA[3:0]	CMD[3:0]	RD1[7:0]	RD[7:0]	CRC[7:0]

Table 138. Command and response mode – field definitions

Field	Length (bits)	Definition
PA[3:0]	4	Physical address Matches the value in the PADDR[3:0] of the PHYSADDR register
CMD[3:0]	4	An echo of the received command
ED[7:0]	8	The data contained in the register addressed by RA[7:1] + 1 (see Section 11.2.3.4 "DSI3 command and response mode command summary")
RD[7:0]	8	The data contained in the register addressed by RA[7:1] + 0 (see Section 11.2.3.4 "DSI3 command and response mode command summary")
CRC[7:0]	8	Error checking (see Section 11.2.3.2.3 "Error checking")

11.2.3.2.3 Error checking

The device calculates a CRC on the entire 32 bits of each response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC encoding procedure is:

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1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed for command and response mode are shown in Table 139.

Table 139. Command and response mode response CRC

Mode	Default polynomial	Seed
Command and response	$x^8 + x^5 + x^3 + x^2 + x + 1$	1111 1111

Some example CRC calculations are shown in Section 11.2.3.1.3 "Error checking".

11.2.3.3 DSI3 command and response mode timing

A timing diagram for command and response mode is shown in Figure 38. Timing parameters are specified in Section 10 "Dynamic characteristics".

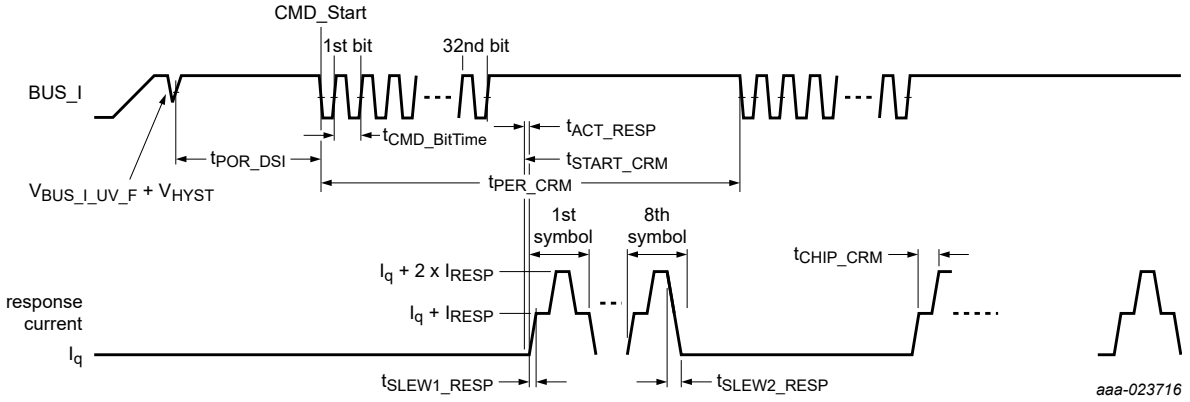


Figure 38. Command and response mode timing diagram

11.2.3.4 DSI3 command and response mode command summary

Command						Data														
C3	C2	C1	C0	Hex	Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	$0	Register read	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	x	x	x	x	x	x	x	x	x
0	0	0	1	$1	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	0	1	0	$2	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	0	1	1	$3	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	0	0	$4	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	0	1	$5	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	1	0	$6	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	1	1	$7	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	0	0	$8	Register write	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]
1	0	0	1	$9	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	1	0	$A	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	1	1	$B	Enter PDCM	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	0	$C	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	1	$D	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

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Command						Data															
C3	C2	C1	C0	Hex	Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	$E	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	1	1	$F	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

11.2.3.4.1 Register read command

The device supports the register read command as a device address specific command only. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register and a valid CRC is calculated, the device responds to the command.

The device ignores the register read command if the command is sent to any other physical address, including the DSI global device address of 0000.

The register read command uses the byte address definitions shown in Section 6.1 "User accessible data array". The register read response includes the register contents at the time the register read command decode is complete. Readable registers along with their byte addresses are shown in Section 6.1 "User accessible data array". If an attempt is made to read a register that is not readable, the device will respond with all zero data.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	0	0	0	0	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	x	0	0	0	0	0	0	0	0	8 bits

Table 140. Register read command format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored.
C[3:0]	Register read command = 0000
RA[7:1]	RA[7:1] contains the upper 7 bits of the byte address for the register to be read.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	0	0	0	0	RD [15]	RD [14]	RD [13]	RD [12]	RD [11]	RD [10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Table 141. Register read command: response format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Register read command = 0000
RD[15:8]	The data contained in the register addressed by RA[7:1] + 1
RD[7:0]	The data contained in the register addressed by RA[7:1] + 0

A register read command to a register address outside the addresses listed in Section 6.1 "User accessible data array" will result in a valid response. The data for the registers will be 0000h.

11.2.3.4.2 Register write command

The device supports the register write command as a device address specific command. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will execute the register write and respond to the command.

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The device ignores the register write command if the command is sent to any other physical address, including the DSI global device address of 0000, with one exception as explained in Section 11.2.3.4.3 "Global register write command to the PHYSADDR register".

The register write command uses the byte address definitions shown in Section 6.1 "User accessible data array". Writable registers along with their byte addresses are shown in Section 6.1 "User accessible data array".

Address				Command				Data														CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA [3]	PA [2]	PA [1]	PA [0]	1	0	0	0	RA [7]	RA [6]	RA [5]	RA [4]	RA [3]	RA [2]	RA [1]	RA [0]	RD [7]	RD [6]	RD [5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Table 142. Register write command format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored.
C[3:0]	Register write command = 1000
RA[7:0]	RA[7:0] contains the byte address of the register to be read.
RD[7:0]	RD[7:0] contains the data to be written to the register addressed by RA[7:0].

Address				Command				Data														CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	0	RD [15]	RD [14]	RD [13]	RD [12]	RD [11]	RD [10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Table 143. Register write command: response format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Register write command = 1000
RD[15:8]	The data contained in the register addressed by RA[7:1] + 1 (after the register write is executed)
RD[7:0]	The data contained in the register addressed by RA[7:1] + 0 (after the register write is executed)

A register write command to a register address outside the addresses listed in Section 6.1 "User accessible data array" will not execute, but will result in a valid response. The data for the registers will be 0000h.

A register write command to a read-only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

11.2.3.4.3 Global register write command to the PHYSADDR register

The device supports the register write command as a global address under the following conditions:

1. The register write command is written to the PHYSADDR register.
2. The PADDR[3:0] bits of the PHYSADDR register are equal to '0000' prior to the register write being executed.

If these conditions are met, the device will execute the register write and respond to the command.

Address				Command				Data														CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

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Table 144. Global register write command format

Bit field	Definition
PA[3:0]	The DSI global address of 0000
C[3:0]	Register write command = 1000
RA[7:0]	RA[7:0] must be set to the PHYSADDR register address.
RD[3:0]	RD[3:0] contains the new physical address for the device.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	0	RD [15]	RD [14]	RD [13]	RD [12]	RD [11]	RD [10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	8 bits

Table 145. Global register write command – response format

Bit field	Definition
PA[3:0]	The new DSI physical address programmed to the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Register write command = 1000
RD[15:8]	The data contained in register after PHYSADDR
RD[7:0]	The data contained in the PHYSADDR register after the register write is executed.

11.2.3.4.4 Enter periodic data collection mode command

The device supports an enter PDCM command as a device address specific command and as a global command.

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will set the ENDINIT bit in the DEVLOCK_WR register, enter periodic data collection mode, and respond to the command as shown below. If the PA[3:0] field in the command matches the global address of '0000', the device will set the ENDINIT bit in the DEVLOCK_RW register and enter periodic data collection mode regardless of the value of the PADDR[3:0] bits in the PHYSADDR register (this includes PADDR = 0h). No response is transmitted for a global command. The device ignores the enter PDCM command if the command is sent to any other physical address.

The various DSI3 communication modes are controlled by the PDCM enable command and the BDM_EN bit in the BDM_CFG register as shown below:

eDCM Enabled	BDM_EN	Command and response mode	Periodic data collection mode	Background diagnostic mode
No	0	Enabled	Disabled	Disabled
No	1	Enabled	Disabled	Disabled
Yes	0	Disabled	Enabled	Disabled
Yes	1	Disabled	Enabled	Enabled

Once the ENDINIT bit is set, the registers listed in Section 6.3.3 "OTP modifiable registers" are locked and the user array read/write register array verification is enabled. The ENDINIT bit can only be cleared by a device reset.

Address				Command				Data																CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8 bits

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Table 146. Enter periodic data collection mode command format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register or the global address of '0000'. Otherwise, the command is ignored.
C[3:0]	Enter PDCM command = 1011

Address				Command				Data															CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	1	0	1	1	0	0	0	0	Ch[3]	Ch[2]	Ch[1]	Ch[0]	0	0	0	0	0	0	0	0	8 bits

Table 147. Enter periodic data collection mode command: response format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
Ch[3:0]	CHIPTIME[3:0] in the CHIPTIME register
C[3:0]	Enter periodic data collection mode command = 1011

11.2.3.4.5 Reserved commands

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register and a valid CRC is calculated, the device will respond to reserved commands. The physical address and command will be echoed and the correct CRC will be transmitted. The data included in the response is undefined.

Address				Command				Data															CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits
PA[3]	PA[2]	PA[1]	PA[0]	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits

Table 148. Reserved commands

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored.
C[3:0]	Invalid commands
x	Don’t care

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Address				Command				Data															CRC
PA3	PA2	PA1	PA0	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
PA[3]	PA[2]	PA[1]	PA[0]	C[3]	C[2]	C[1]	C[0]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	8 bits

Table 149. Reserved command response format

Bit field	Definition
PA[3:0]	DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register.
C[3:0]	Reserved command echo

11.2.4 DSI3 periodic data collection mode and background diagnostic mode

When the ENDINIT bit in the DEVLOCK_WR register is set, periodic data collection mode is enabled and the optional background diagnostic mode is enabled.

11.2.4.1 DSI3 periodic data collection mode and background diagnostic mode command reception

When periodic data collection mode is enabled, the device will decode the DSI3 broadcast read command as well as background diagnostic mode command fragments as described below.

11.2.4.1.1 Bit encoding

The command bit encoding for periodic data collection mode and background diagnostic mode is the same as the bit encoding for command and response mode, as described in Section 11.2.3.1.1 "Bit encoding".

11.2.4.1.2 Command message format

The command message format for periodic data collection mode and background diagnostic mode is the same as the command message format for command and response mode, as described in Section 11.2.3.1.2 "Command message format".

If background diagnostic mode is disabled, then the device responds with the periodic data collection mode response only if the command is the single bit broadcast read command. A broadcast read command may be either a '1' or a '0'. Figure 39 shows the broadcast read commands supported by the device.

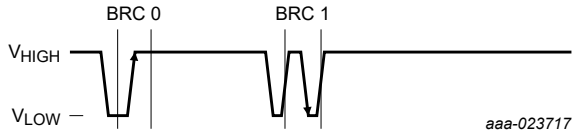


Figure 39. Background diagnostic mode command bit encoding

If background diagnostic mode is enabled:

- Background diagnostic mode commands are transmitted and decoded in 2-bit or 4-bit fragments depending on the state of the BDM_FRAGSIZE bit in the BDM_CFG register.
- The device responds with the periodic data collection mode response if and only if the command is a broadcast read command or a command fragment.
- A broadcast read command or any command length other than 2 or 4 bits resets the background diagnostic mode command decode.
- The device responds with a background diagnostic mode response only when a full 32-bit command is received and the decoded command is a valid command and response mode command.

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See Section 11.2.4.4 "Background diagnostic mode response transmission" for additional details on background diagnostic mode timing.

11.2.4.1.3 Error checking

The error checking for background diagnostic mode commands is the same as the error checking for command and response mode, and described in Section 11.2.3.1.3 "Error checking".

No error checking is employed for the broadcast read commands.

11.2.4.2 DSI3 periodic data collection mode response transmission

When periodic data collection mode is enabled and the device receives either a broadcast read or background diagnostic command, the device will respond with periodic data as shown in Figure 40 and described in Section 11.2.4.2.1 "Symbol encoding", Section 11.2.4.2.2 "Response message format", and Section 11.2.4.2.3 "Error checking"..

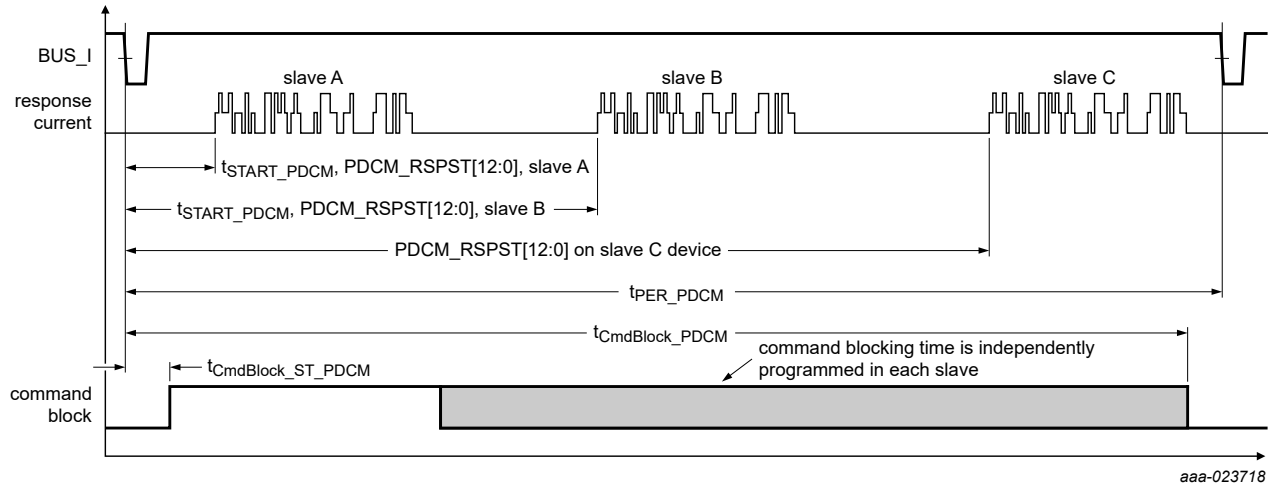


Figure 40. Periodic data mode response transmission

11.2.4.2.1 Symbol encoding

The symbol encoding used for periodic data collection mode responses is the same as for command and response mode responses, and described in Section 11.2.3.2.1 "Symbol encoding".

11.2.4.2.2 Response message format

The periodic data collection mode response format is shown below. Field sizes are defined by the PDCMFORMAT[2:0] bits in the SOURCEID_x register in Section 6.2.12 "SOURCEID_x – source identification registers (address $1A, $1B)".

Source ID	Keep alive counter	Status	Sensor data	CRC
SOURCEID	KAC	S	D	CRC[7:0]

- If enabled in the PDCMFORMAT[2:0] bits, the SOURCEID field includes the value stored in the SOURCEID_x[3:0] bits of the SOURCEID_x register.
- If enabled in the PDCMFORMAT[2:0] bits, the keep alive counter field is a 2-bit rolling message counter that is independently incremented for each SOURCEID. The initial value of the counter is '00'.

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- If enabled, the status field is transmitted as listed in Section 11.2.4.2.2 "Response message format". See Section 11.2.7 "DSI3 exception handling" for details on exception handling.
- The sensor data field includes the sensor data as selected by the DATATYPEx bits for the SOURCEID.
- The CRC field includes an 8-bit CRC as defined in Section 11.2.4.2.3 "Error checking".

Table 150. Periodic data collection mode status field definition

s[3:0]				Description	DEVSTAT state	SUP_ERR_DIS state	Error priority	Sensor data field value	
								STATUS field size = 4	STATUS field size = 0
0	0	0	0	Normal mode	N/A	N/A	16	Sensor data	
0	0	0	1	Normal mode, user array not locked (UF2 region has not been locked)	N/A	N/A	15	Sensor data	The sensor data field error code is transmitted for a minimum of one transmission
0	0	1	0	Self-test incomplete or self-test active or self-test error present	Bit set in DSP_STAT: ST_INCMPLT or ST_ACTIVE or ST_ERROR	N/A	14	Sensor data	The sensor data field error code is transmitted for a minimum of one transmission
0	0	1	1	Oscillator training error	Bit set in DEVSTAT3	N/A	13	Sensor data	The sensor data field error code is transmitted for a minimum of one transmission
0	1	0	0	PABS out of range error	Bit set in DSP_STAT: PABS_HIGH or PABS_LOW or PABS_MISMATCH	N/A	12	Sensor data	The sensor data field error code is transmitted for a minimum of one transmission
0	1	0	1	Temperature error	Bit set in DEVSTAT2	N/A	11	Sensor data	The sensor data field error code is transmitted for a minimum of one transmission
0110 to 0111				Reserved	N/A	N/A	9.10	Sensor data	The sensor data field error code is transmitted for a minimum of one transmission
1	0	0	0	User OTP memory error (UF2)	U_OTP_ERR set in DEVSTAT2	N/A	8	The sensor data field error code is transmitted for a minimum of one transmission	
1	0	0	1	User R/W memory error (UF2)	U_RW_ERR set in DEVSTAT2	N/A	7	The sensor data field error code is transmitted for a minimum of one transmission	
1	0	1	0	NXP OTP memory error	F_OTP_ERR set in DEVSTAT2	N/A	6	The sensor data field error code is transmitted for a minimum of one transmission	
1	0	1	1	Test mode active	TESTMODE bit set in DEVSTAT	N/A	5	The sensor data field error code is transmitted for a minimum of one transmission	
1	1	0	0	Supply error	Bit set in DEVSTAT1	0	4	No response until the supply monitor timer expires. The sensor data field error code is transmitted for a minimum of one transmission (See Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)")	
						1		No response until the supply monitor timer expires. (See Section 6.2.2 "DEVSTATx – device status registers (address $01-$04)")	
1	1	0	1	Reset error	DEVRES Set	N/A	3	The sensor data field error code is transmitted for a minimum of one transmission	
1110 to 1111				Reserved	N/A	N/A	1,2	The sensor data field error code is transmitted for a minimum of one transmission	

Note: *If any data source is configured for signed data, all error code transmissions will use the signed data error code.*

11.2.4.2.3 Error checking

The device calculates a CRC on the entire response. Message data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.

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3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial and seed for periodic data collection mode are shown in Table 151.

Table 151. Periodic data collection mode response CRC

Mode	Default polynomial	Nondirect seed
Periodic data collection mode	$x^8 + x^5 + x^3 + x^2 + x + 1$	0000, SOURCEID_x[3:0]

Some example CRC calculations are shown in Table 152.

Table 152. Periodic data collection mode – CRC calculation examples

Source identification (4 bits)	Keep alive counter (2 bits)	Status (4 bits)	Sensor data (10 bits)	Nondirect seed	8-bit CRC
1h	3h	0h	1FFh	01h	D6h
2h	2h	0h	1FEh	02h	70h
3h	1h	0h	20Dh	03h	B0h
4h	0h	0h	1EAh	04h	5Fh

11.2.4.3 DSI3 periodic data collection mode timing

A timing diagram for periodic data collection mode is shown in Figure 41. Timing parameters are specified in Section 10 "Dynamic characteristics".

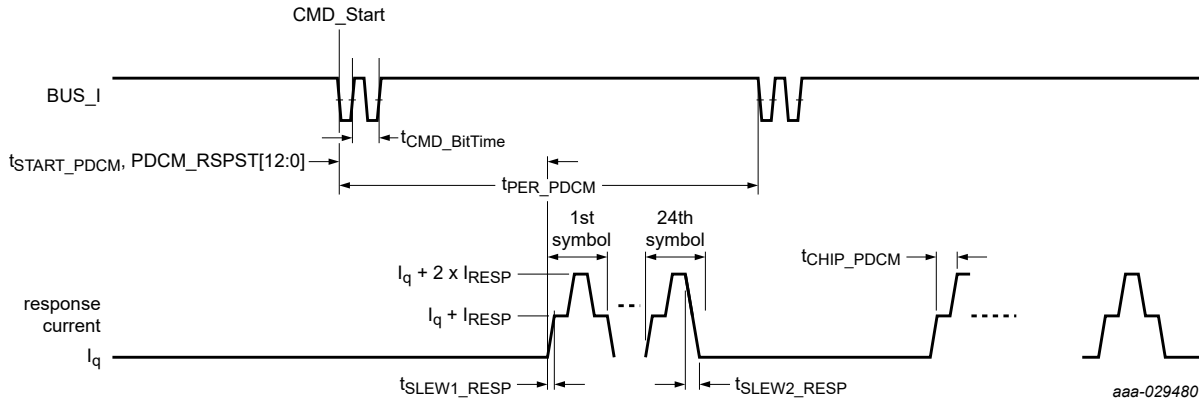


Figure 41. Periodic data collection mode timing diagram

11.2.4.4 Background diagnostic mode response transmission

11.2.4.4.1 Symbol encoding

The background diagnostic mode response symbol encoding is the same as the symbol encoding used for command and response mode responses and is described in Section 11.2.3.2.1 "Symbol encoding".

11.2.4.4.2 Response message format

The background diagnostic mode response message format is the same as the format used for command and response mode responses and is described in Section 11.2.3.2.2 "Response message format".

- If a complete, 32-bit command is received, and decoded to a valid command and response mode command, the device provides a background diagnostic mode response.

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- Responses are initiated by the master transmitting 1-bit broadcast read commands following a completed background diagnostic mode command transmission.
- Responses are transmitted in one or two symbol fragments (depending on the state of the BDM_FRAGSIZE bit) following the 1-bit broadcast read command, using the same timing window within the frame that the background diagnostic mode command used.
- Responses are transmitted if and only if broadcast read commands are received.
- Four or eight consecutive broadcast read commands are required following a valid background diagnostic mode command to complete a response transmission (depending on the state of the BDM_FRAGSIZE bit).
- If any command other than the broadcast read command is received, no response is transmitted and the remainder of the broadcast read command response is terminated.
- The data to be transmitted in the response is latched just before the first symbol of the background diagnostic mode response.

See Section 11.2.4.5 "DSI3 background diagnostic mode timing" for background diagnostic mode timing.

11.2.4.4.3 Error checking

The error checking for background diagnostic mode responses is the same as used for command and response mode, and described in Section 11.2.3.1.3 "Error checking".

11.2.4.5 DSI3 background diagnostic mode timing

An example timing diagram for background diagnostic mode is shown in Figure 42. In this example, BDM_FRAGSIZE is set to '1' (4 bits). Timing parameters are specified in Section 10 "Dynamic characteristics".

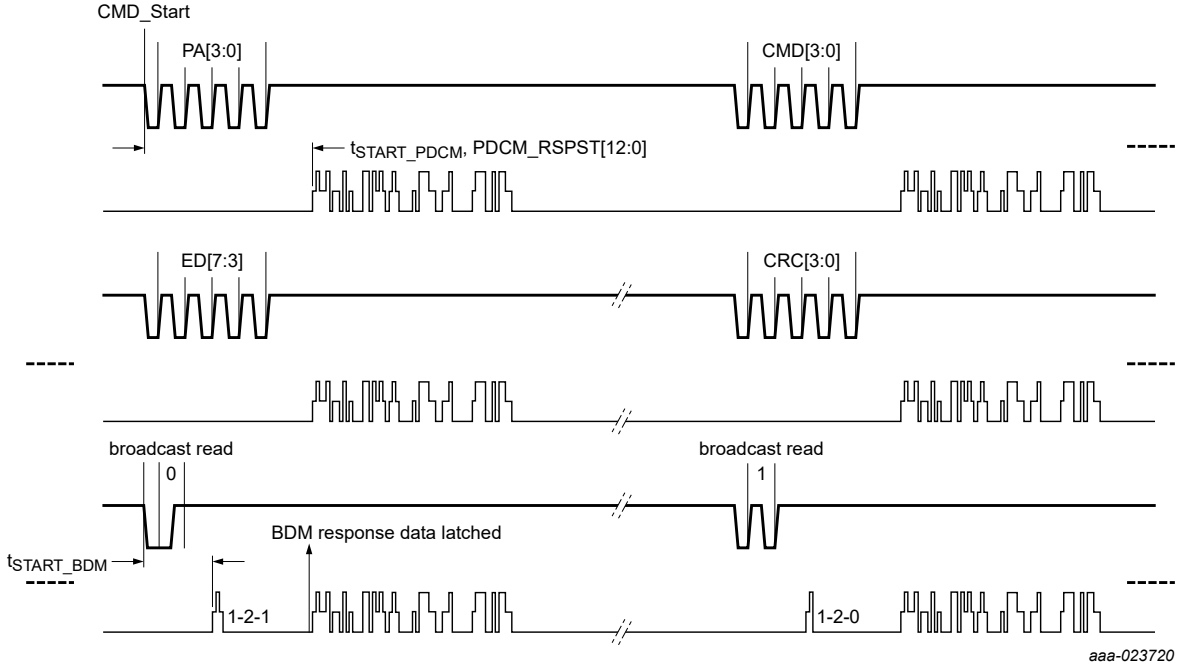


Figure 42. Background diagnostic mode timing diagram

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11.2.4.6 DSI3 periodic data collection mode and background diagnostic mode command summary

When periodic data collection mode is enabled, the background diagnostic mode supports the register read command as described in the command and response mode command summary, Section 11.2.3.4.1 "Register read command". The register write command is not supported in background diagnostic mode.

11.2.4.7 DSI3 PDCM data transmission modes

11.2.4.7.1 Simultaneous sampling mode (SS_EN = 1)

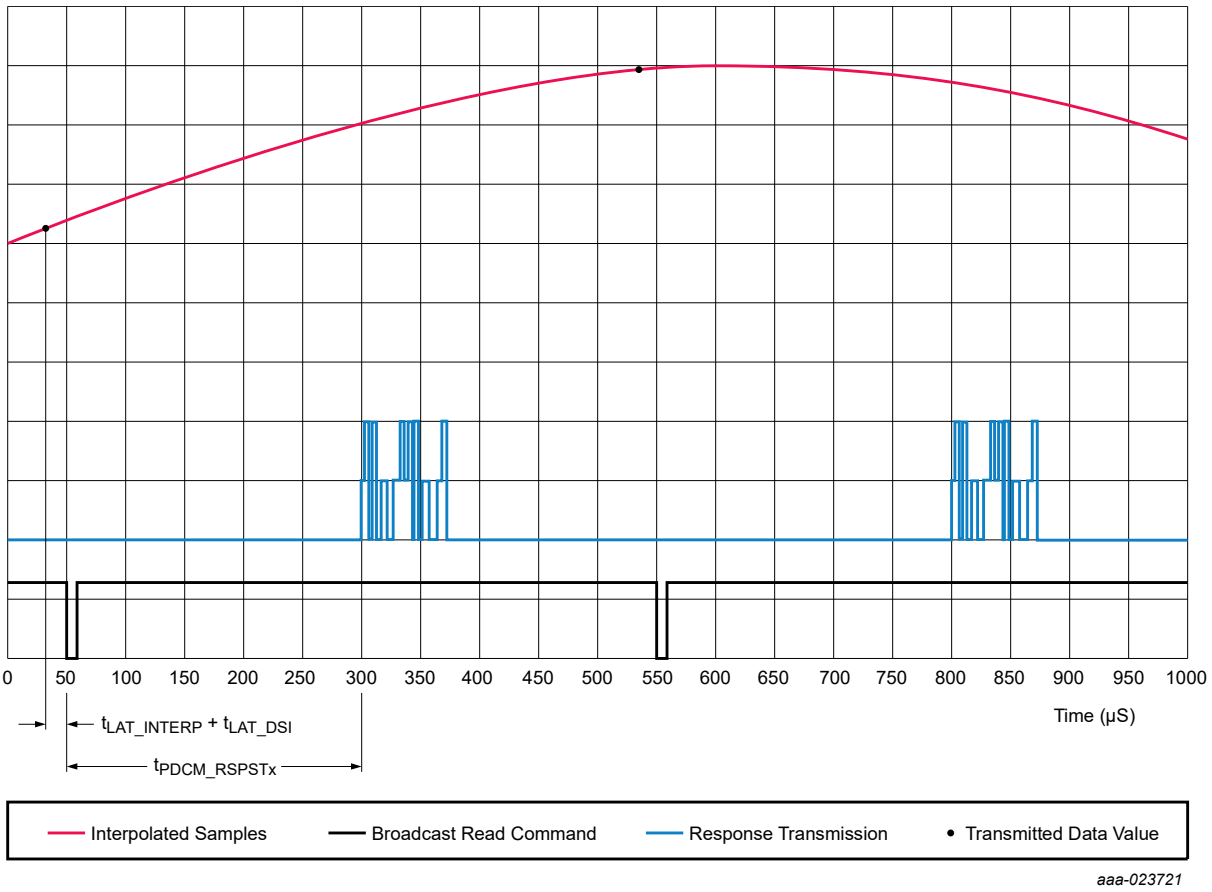


Figure 43. Simultaneous sampling mode

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11.2.4.7.2 Synchronous sampling mode with minimum latency (SS_EN = 0)

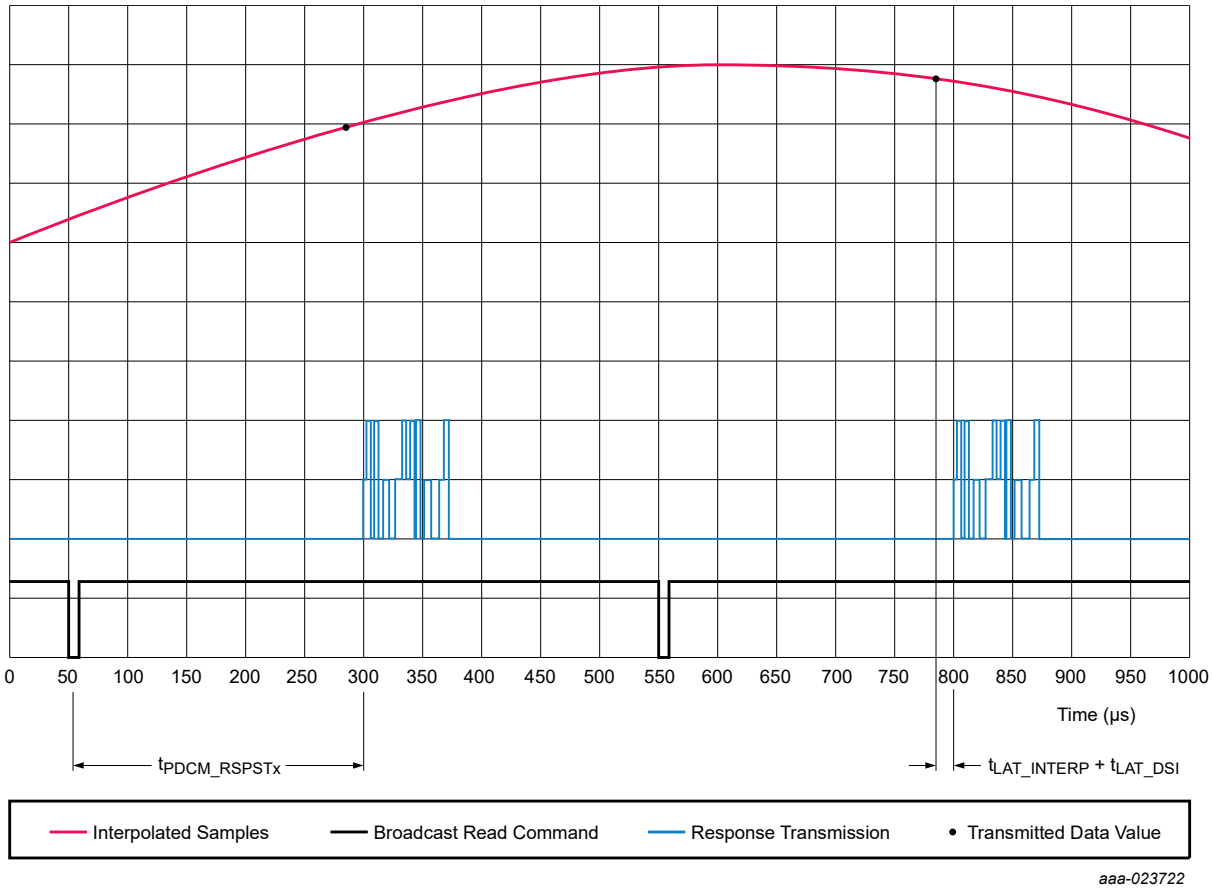


Figure 44. Synchronous sampling mode with minimum latency

11.2.5 Initialization timing

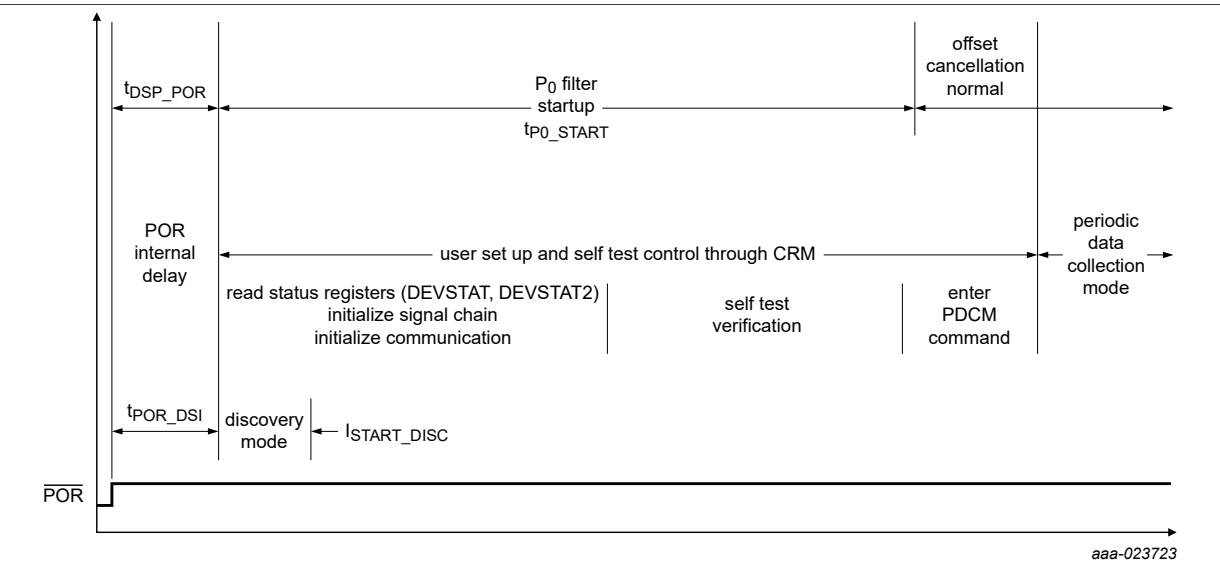


Figure 45. Initialization timing

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11.2.6 Maximum number of devices on a network

The theoretical maximum number of devices on a DSI3 network is 16: 1 master and 15 slaves. The practical limit for the number of devices on a bus is dependent on the minimum common capability of the devices on the bus. The capability of the device is different depending on the bus configuration and operating mode. The impact of the device capability on the practical limit for the number of devices on the network is described in Section 11.2.6.1 "Preconfigured, parallel connected network", Section 11.2.6.2 "Bus switch connected daisy chain network", and Section 11.2.6.3 "Resistor connected daisy chain network using discovery mode".

11.2.6.1 Preconfigured, parallel connected network

The number of devices in a preconfigured, parallel connected network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.

11.2.6.2 Bus switch connected daisy chain network

The number of devices in a bus switch connected daisy chain network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The current handling capability and resulting voltage drop of the external bus switches in the network.

11.2.6.3 Resistor connected daisy chain network using discovery mode

The number of devices in a resistor connected daisy chain network is limited by the capability of the device. The maximum number of equivalent devices connected to the BUS_O pin of a device is three. This is limited by the total quiescent current drawn from the BUS_O pin during discovery mode ($I_{BUS_O_q}$).

The practical limit is determined by a combination of the above restriction and the following:

- The capability of the master device, including, but not limited to:
  - The bus operating voltage
  - The bus supply current
  - The bus current limit
  - The bit rate
  - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The maximum allowed quiescent current drawn from the BUS_O pin of other slaves in the system.
- The resulting voltage drop of the Discovery mode resistors in all slaves in the network.

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11.2.7 DSI3 exception handling

Table 153 summarizes the exception conditions detected by the device and the response for each exception.

Table 153. DSI3 exception handling

Condition		Description	Device response
Exception	**PDCM enabled**		
power-on-reset	N/A	Power Applied	• See Section 11.2.5 • ST_INCMPLT set, PDCM disabled. The device must be reinitialized
V_{BUS_I} error	N/A	$V_{BUS_I} < V_{BUS_I_UV_F}$	• Response current deactivated • BUSIN_UV_ERR set, PDCM Status set as specified in Section 11.2.4.2.2 • The device ignores commands in CRM
V_{BUF} error	N/A	$V_{BUF} < V_{BUF_UV_F}$	• Response current deactivated • VBUFUV_ERR set, PDCM Status set as specified in Section 11.2.4.2.2 • The device ignores commands in CRM
Internal regulator error	N/A	Internal regulator undervoltage condition	• The device is held in reset • No response to DSI commands • If activated, BUSSW_L or BUSSW_H is deactivated • The device must be reinitialized when the internal regulator returns above the threshold
OTP error detection fault (Factory array)	N/A	Error detected in factory programmed OTP array.	• Periodic data collection mode response data set to error response • F_OTP_ERR set, PDCM Status set as specified in Section 11.2.4.2.2
OTP error detection fault (User array)	N/A	Error detected in user programmed OTP array and the LOCK_U bit is set.	• Periodic data collection mode response data set to error response • U_OTP_ERR set, PDCM Status set as specified in Section 11.2.4.2.2
User R/W array error detection fault	No	N/A	N/A
	Yes	Error detected in user read write registers and the ENDINIT bit is set.	• Periodic data collection mode response data set to error response • U_RW_ERR set, PDCM status set as specified in Section 11.2.4.2.2
Self-test activated	No	ST activated during initialization	• Internal self-test circuitry enabled • Self-test activation incomplete status cleared • Sensor data registers (SNSDATAx_x) contain self-test active data • ST_ACTIVE set
	Yes	ST activated in periodic data collection mode	• Periodic data collection mode sensor response data normal • Self-test activation ignored
Self-test never activated after POR	No	In initialization, before self-test	• Normal responses to command and response mode
	Yes	In PDCM, self-test incomplete	• Periodic data collection mode sensor response data normal • ST_INCMPLT set, PDCM status set as specified in Section 11.2.4.2.2

11.2.7.1 Daisy chain and discovery mode error handling

Table 154 shows the effect of internal failure modes on the discovery and daisy chain initialization procedures.

Table 154. DSI3 error handling – discovery mode and daisy chain mode

Error condition	Effect on discovery mode	Effect on daisy chain
Supply error	Discovery commands ignored The device will not participate in discovery mode	Daisy chain commands Ignored The device will not participate in daisy chain
Memory error	No effect The device will attempt to participate in discovery mode as programmed	No effect The device will attempt to participate in daisy chain as programmed
Temperature error	No effect The device will attempt to participate in discovery mode as programmed	No effect The device will attempt to participate in daisy chain as programmed
Communication error (internal)	No effect The device will participate in discovery mode as programmed	No effect The device will participate in daisy chain as programmed
PABS out of range error	No effect The device will participate in discovery mode as programmed	No effect The device will participate in daisy chain as programmed
Self-test incomplete or self-test active	Not applicable	Not applicable
Device not locked	No effect The device will participate in discovery mode as programmed	No effect The device will participate in daisy chain as programmed

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11.3 PSI5 protocol

11.3.1 Communication interface overview

The communication interface between a master device and this slave device in PSI5 mode is established via a PSI5 compatible two-wire interface, with parallel or serial (daisy chain) connections to the satellite modules. Figure 46 shows one possible system configuration for multiple satellite modules in parallel.

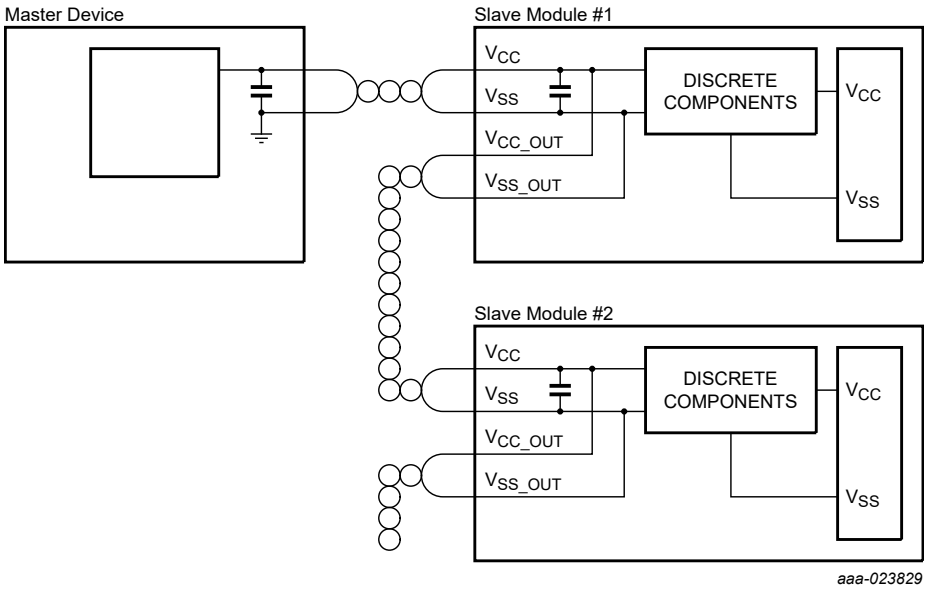


Figure 46. PSI5 satellite interface diagram

11.3.2 Data transmission physical layer

This device uses a two-wire interface for both its power supply (V_{CC}), and data transmission. The PSI5 master supplies a preregulated voltage to this device. Data transmissions and synchronization control from the PSI5 master to this device are accomplished via modulation of the supply voltage. Data transmissions from this device to the PSI5 master are accomplished via modulation of the current on the power supply line.

11.3.2.1 Synchronization pulse

The PSI5 master modulates the supply voltage in the positive direction to provide synchronization of the satellite sensor data. Upon reception of a synchronization pulse, the device delays a specified period of time, called a time slot, before transmitting sensor data. For more details regarding time slots, refer to Section 6.2.17 "PDCM_RSPSTx_x – DSI3 and PSI5 start time registers (address $26 to $29)" and Section 10 "Dynamic characteristics".

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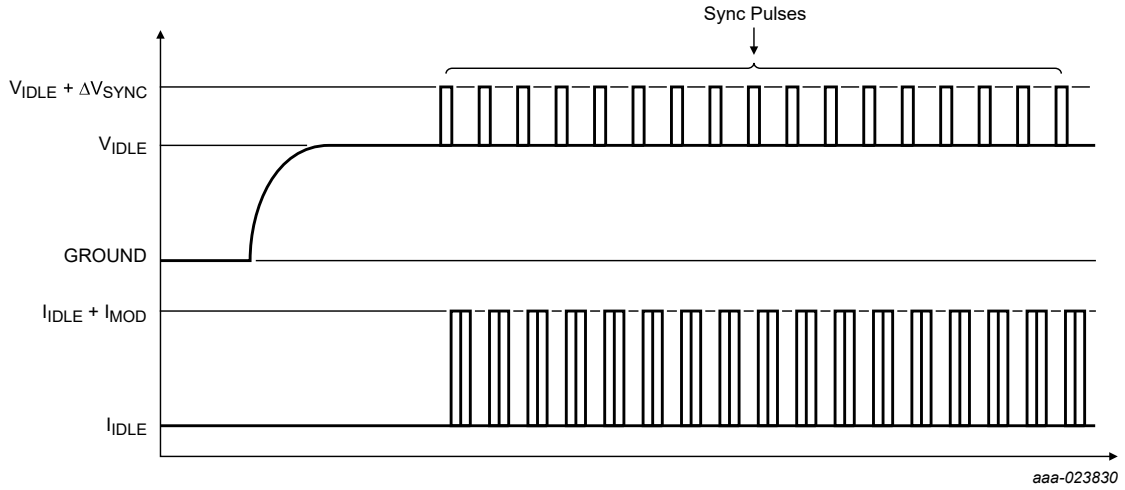


Figure 47. Synchronous communication overview

11.3.2.1.1 Synchronization pulse detection

The synchronization (sync) pulse detection block generates a valid synchronization pulse signal following the detection of an externally generated sync pulse. This signal resets the sync pulse time reference (t_{TRIG}), and initiates the timers associated with response messages.

The supply voltage can vary throughout the specified range, so the external sync pulses may have different absolute voltage levels. Thus, the sync pulse detection threshold (V_{CC_SYNC}) is dependent not only on the sync pulse absolute voltage, but also on the supply voltage. Figure 48 shows a block diagram of the sync pulse detection circuit.

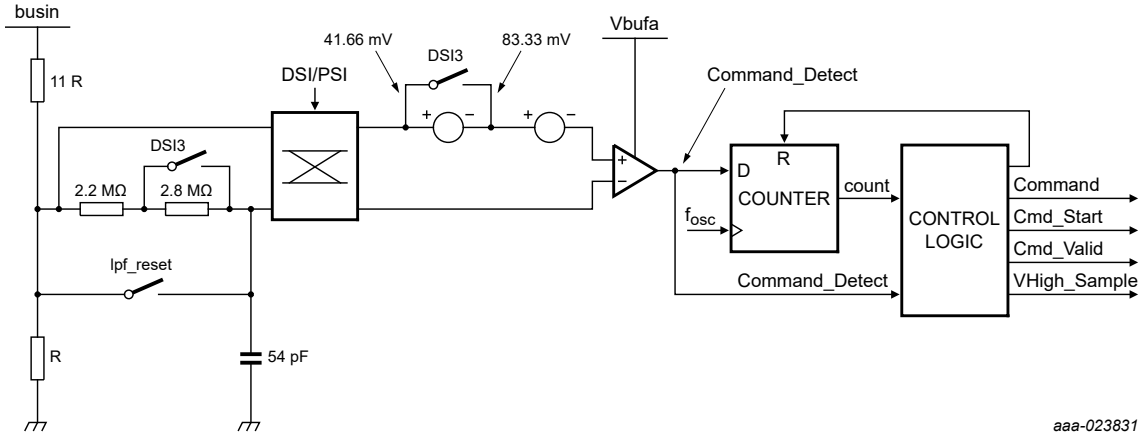


Figure 48. Synchronization pulse detection circuit

The start of a sync pulse is detected when the comparator output is set. The comparator output is input into a counter, and the counter is updated at a fixed frequency. At a fixed time after the initial sync pulse detection, the counter is compared against a limit (the minimum value of t_{SYNC}). If the counter is above the limit, a valid sync pulse is detected.

If the sync pulse is valid, the following occur:

1. The valid sync pulse detection signal is set.
2. The detection counter is reset and disabled for t_{SYNC_OFF} (referenced from t_{TRIG}). t_{SYNC_OFF} can be programmed by the user via the PDCM_CMD_B_x registers. See Section 6.2.18 "PDCM_CMD_B_x – DSI3

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and PSI5 command blocking time registers (address $38, $39)" for details on the programmable option and Section 10 "Dynamic characteristics" for timing specifications for each option.

3. The sync pulse detection low-pass filter is reset for a specified time ($t_{SYNC_LPF_RESET}$).

If the sync pulse is invalid, all timers are reset, and the detector becomes sensitive for the very next f_{SYNC_DET} sample.

The output of the comparator is monitored at the SampCLK frequency. Once the comparator output goes high, all of the internal timers are started, so that the t_{TRIG} jitter is minimized.

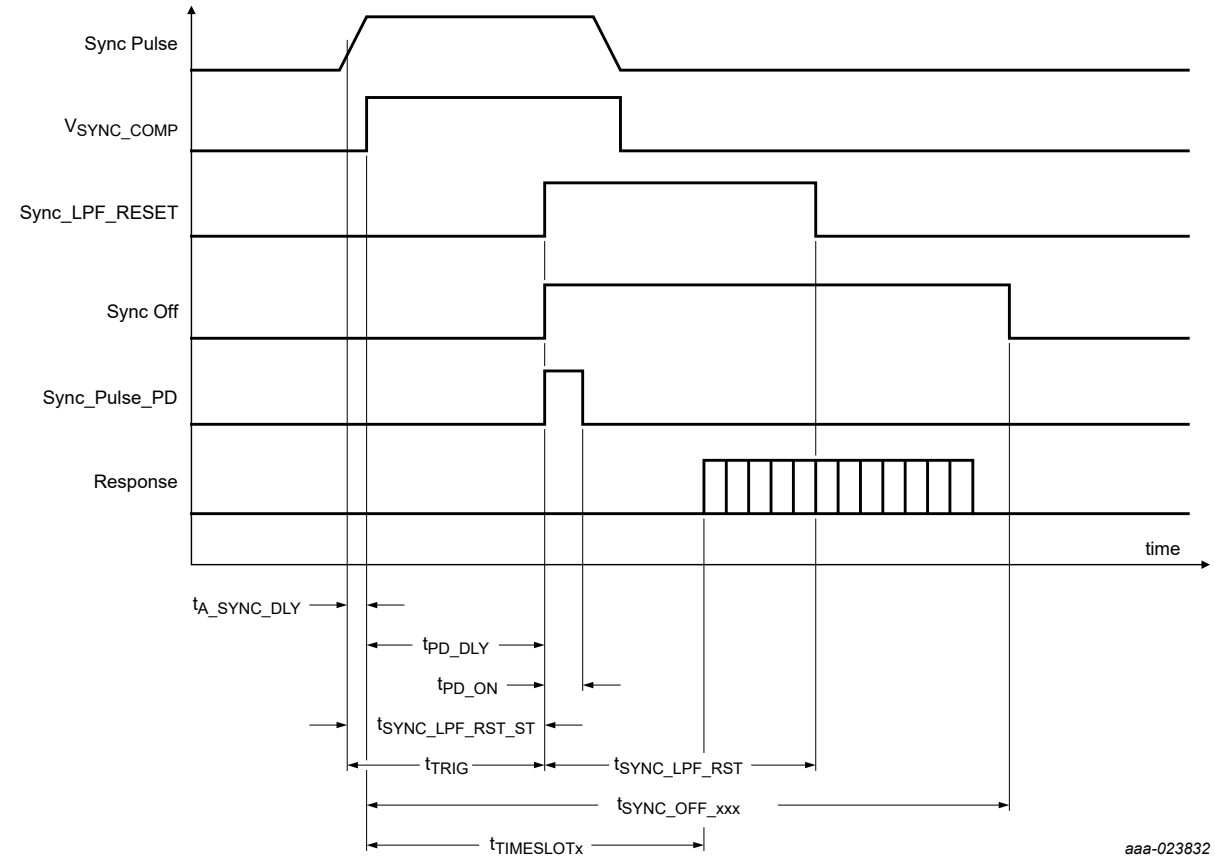


Figure 49. Synchronization pulse detection timing

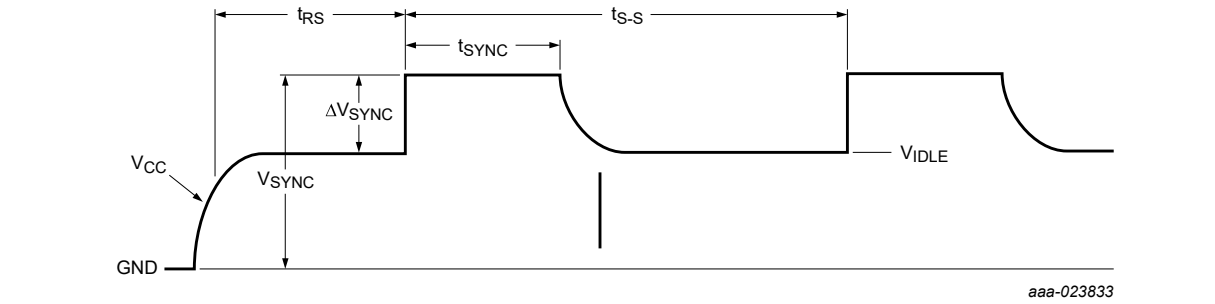


Figure 50. Sync pulse characteristics

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11.3.2.1.2 Synchronization pulse pulldown function

The device includes an optional sync pulse pulldown function for systems in which the master device does not include an active pulldown function. The device uses the modulation current pulldown circuit, which sinks I_{MOD} – I_{IDLE} additional current from the BUS_I pin. The pulldown current is activated after t_{PD_DLY} (referenced to t_{TRIG}), and is activated for t_{PD_ON}.

The sync pulse pulldown function is disabled in programming mode, in initialization phase 1, and in daisy chain mode until the run command is received.

11.3.3 Data transmission data link layer

11.3.3.1 Bit encoding

The device outputs data by modulation of the V_{CC} current using Manchester encoding. Data is stored in a transition occurring in the middle of the bit time. The signal idles at the normal quiescent supply current. A logic low is defined as an increase in current at the middle of a bit time. A logic high is defined as a decrease in current at the middle of a bit time. There is always a transition in the middle of the bit time. If consecutive '1' or '0' data are transmitted, There will also be a transition at the start of a bit time.

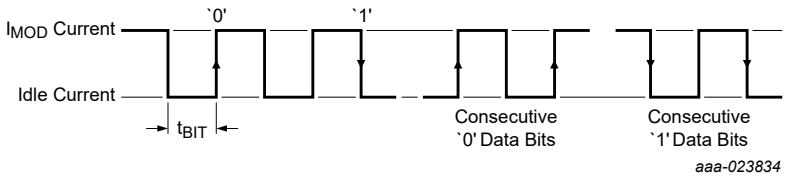


Figure 51. Manchester data bit encoding

11.3.3.2 PSI5 data transmission

PSI5 data transmission frames are composed of two start bits, a 10-bit data word, and error detection bit(s). Data words are transmitted least significant bit (LSB) first. A typical Manchester encoded transmission frame is illustrated in Figure 52.

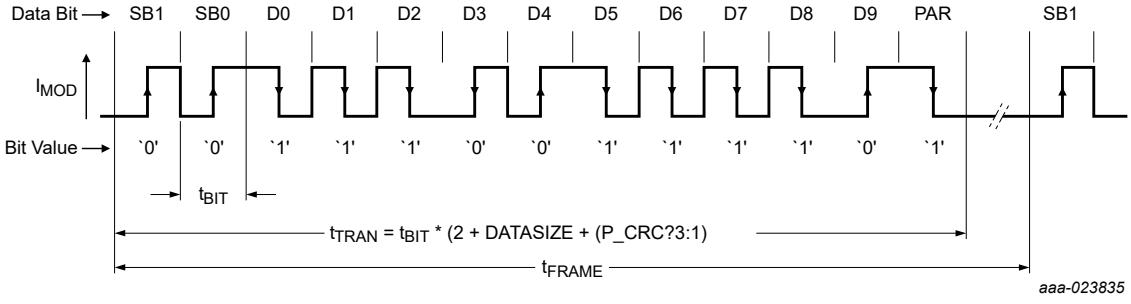


Figure 52. Example Manchester encoded data transfer – psi5-x10x

11.3.3.3 Error detection

Error detection of the transmitted data is accomplished via either a parity bit, or a 3-bit CRC. The type of error detection used is selected by the P_CRC bit in the PSI5_CFG register.

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11.3.3.3.1 Parity error detection

When parity error detection is selected, even parity is employed. The number of logic '1' bits in the transmitted message must be an even number.

11.3.3.3.2 3-bit CRC error detection

When CRC error detection is selected, a 3-bit CRC is appended to each response message. The 3-bit CRC uses a generator polynomial of $g(x) = x^3+x+1$, with a nondirect seed value = '111'. Message data from the transmitted message is read into the CRC calculator LSB first, and the data is augmented with three '0's. Start bits are not used in the CRC calculation. Table 155 shows some example CRC calculation values for 10-bit data transmissions.

Table 155. PSI5 3-bit CRC calculation examples

Data transmitted											CRC		
Hex	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C2	C1	C0
000h	0	0	0	0	0	0	0	0	0	0	1	1	0
0CCh	0	0	1	1	0	0	1	1	0	0	0	1	1
151h	0	1	0	1	0	1	0	0	0	1	0	0	0
1E0h	0	1	1	1	1	0	0	0	0	0	0	1	1
1F4h	0	1	1	1	1	1	0	1	0	0	0	1	0
220h	1	0	0	0	1	0	0	0	0	0	1	0	0
275h	1	0	0	1	1	1	0	1	0	1	1	1	1
333h	1	1	0	0	1	1	0	0	1	1	0	0	1
3FFh	1	1	1	1	1	1	1	1	1	1	1	0	0

11.3.3.4 PSI5 data field and data range values

Table 156 shows the details for each data range. The PSI5 data field size is defined by the PDCMFORMAT bits in the SOURCEID_x registers as described in Section 6.2.12 "SOURCEID_x – source identification registers (address $1A, $1B)".

Table 156. PSI5 data values

10-bit data value, DATA_EXT = 0		10-bit data value, DATA_EXT = 1			Description (EMSG_EXT = 1 in PSI5_CFG)	Description (EMSG_EXT = 0 in PSI5_CFG)	P_0 data transmissions in initialization phase 3
Decimal	Hex	Decimal	Binary	Hex			
+511	1FFh	+511	—	1FFh	Reserved	Reserved	—
+510	1FEh	+510	—	1FEh			
+509	1FDh	+509	—	1FDh			
+508	1FCh	+508	—	1FCh			
+507	1FBh	+507	—	1FBh			
+506	1FAh	+506	—	1FAh			
+505	1F9h	+505	—	1F9h			
+504	1F8h	+504	—	1F8h			
+503	1F7h	+503	—	1F7h			
+502	1F6h	+502	—	1F6h			
+501	1F5h	+501	—	1F5h			
+500	1F4h	+500	—	1F4h	Sensor defect error	Sensor defect error	—
+499	1F3h	+499	—	1F3h	Reserved	Reserved	—
+498	1F2h	+498	—	1F2h			
+497	1F1h	+497	—	1F1h			

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Table 156. PSI5 data values*...continued*

10-bit data value, DATA_EXT = 0		10-bit data value, DATA_EXT = 1			Description (EMSG_EXT = 1 in PSI5_CFG)	Description (EMSG_EXT = 0 in PSI5_CFG)	P_0 data transmissions in initialization phase 3
Decimal	Hex	Decimal	Binary	Hex			
+496	1F0h	+496	—	1F0h			
+495	1EFh	+495	—	1EFh	Communication error (OSCTRAIN_ERR bit)	Reserved (error mapped to 1F4h)	—
+494	1EEh	+494	—	1EEh	Test mode enabled (TESTMODE bit set)		
+493	1EDh	+493	—	1EDh	P_{ABS} out of range error (PABS_HIGH, PABS_LOW or PABS_MISMATCH bit set)		
+492	1ECh	+492	—	1ECh	Temperature error (TEMP0_ERR bit set)		
+491	1EBh	+491	—	1EBh	Memory error (F_OTP_ERR, U_OTP_ERR or U_RW_ERR set)		
+490	1EAh	+490	—	1EAh	Sensor self-test error (ST_ERROR bit set)	Sensor self-test error	—
+489	1E9h	+489	—	1E9h	Reserved	Reserved	—
+488	1E8h	+488	—	1E8h	Sensor busy	Sensor busy	—
+487	1E7h	+487	—	1E7h	Sensor ready	Sensor ready	—
+486	1E6h	+486	—	1E6h	Sensor ready, but unlocked	Sensor ready, but unlocked	—
+485	1E5h	+485	—	1E5h	Reserved	Reserved	
+484	1E4h	+484	—	1E4h			
+483	1E3h	+483	—	1E3h			
+482	1E2h	+482	—	1E2h	Bidirectional communication: RC error	Bidirectional communication: RC error	—
+481	1E1h	+481	—	1E1h	Bidirectional communication: RC OK	Bidirectional communication: RC OK	—
+308 to +480	134h to 1E0h		—		Unused	Unused	—
+307	133h	+480	—	1E0h	Maximum positive sensor value	Maximum positive sensor value	—
. . .	. . .	. . .	—	. . .	Positive sensor values	Positive sensor values	—
+3	03h	+3	—	03h			
+2	02h	+2	—	02h			
+1	01h	+1	—	01h			
0	0	0	—	0	Zero[1]	Zero	—
–1	3FFh	–1	—	3FFh	Negative sensor values	Negative sensor values	—
–2	3FEh	–2	—	3FEh			
–3	3FDh	–3	—	3FDh			
. . .	. . .	. . .	—	. . .			—
–102	39Ah	–480	—	220h	Maximum negative sensor value	Maximum negative sensor value	—
–103 to –480	399h to 220h		—		Unused	Unused	—
–481	21Fh	–481	1000011111	21Fh	Initialization data codes 10-bit status data nibble 1 to 16 (0000 to 1111) (Dx)		P_0: D2:D0, in 3 LSBs
. . .	. . .	. . .	. . .	. . .			P_0: D5:D3, in 3 LSBs
–496	210h	–496	1000010000	210h			
–497	20Fh	–497	1000001111	20Fh	Initialization data IDs Block ID 1 to 16 (10-bit mode) (IDx)		P_0: D8:D6, in 3 LSBs
. . .	. . .	. . .	. . .	. . .			P_0: D11:D9, in 3 LSBs
–512	200h	–512	1000000000	200h			

[1] Not equivalent to ΔP/P0 = 0.

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11.3.4 Initialization

Following power up, the device proceeds through an initialization process which is divided into three phases:

- Initialization phase 1: No data transmissions occur
- Initialization phase 2: Sensor self-test and transmission of configuration information
- Initialization phase 3: Transmission of the sensor busy and/or sensor ready/sensor defect messages followed by the P_0 value

Once initialization is completed the device begins normal mode operation, which continues as long as the supply voltage remains within the specified limits.

In asynchronous mode, initialization data is transmitted for source ID 0 only.

In synchronous mode, initialization data is transmitted for each enabled source ID.

In daisy chain mode, initialization data is transmitted in the source ID 0 time slot as defined by the sensor address as documented in Section 11.3.6 "Daisy chain mode".

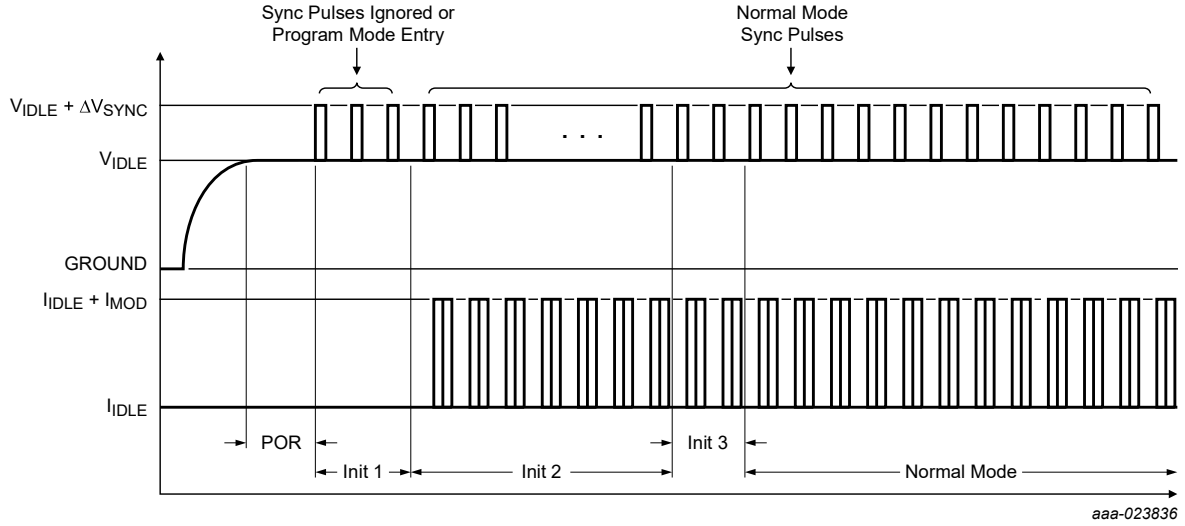


Figure 53. PSI5 sensor 10-bit initialization

During PSI5 initialization, the device completes an internal initialization process consisting of the following:

- Power-on reset
- Device initialization
- Program mode entry verification
- P_0 filter initialization
- Self-test

Figure 54 and Figure 55 show the PSI5 initialization timing, the P0 out of range error is delayed by an internal counter (2 s). The delay is included as an additional mitigation to avoid any unwanted 'out-of-range event' due to a small transient change in P0 around the thresholds. The counter is reset at the start of phase 0, and is not reset depending on the P0 value and continues for 2 seconds. P0 value is compared to the threshold after the counter stops and an error message is transmitted if it is out of range. During normal operation (after the initialization) an error message is transmitted immediately when P0 goes out-of-range.

Figure 54 shows the timing for internal and external initialization in synchronous mode. Figure 55 shows the timing for internal and external initialization in asynchronous mode. Timing parameters are specified in Section 10 "Dynamic characteristics".

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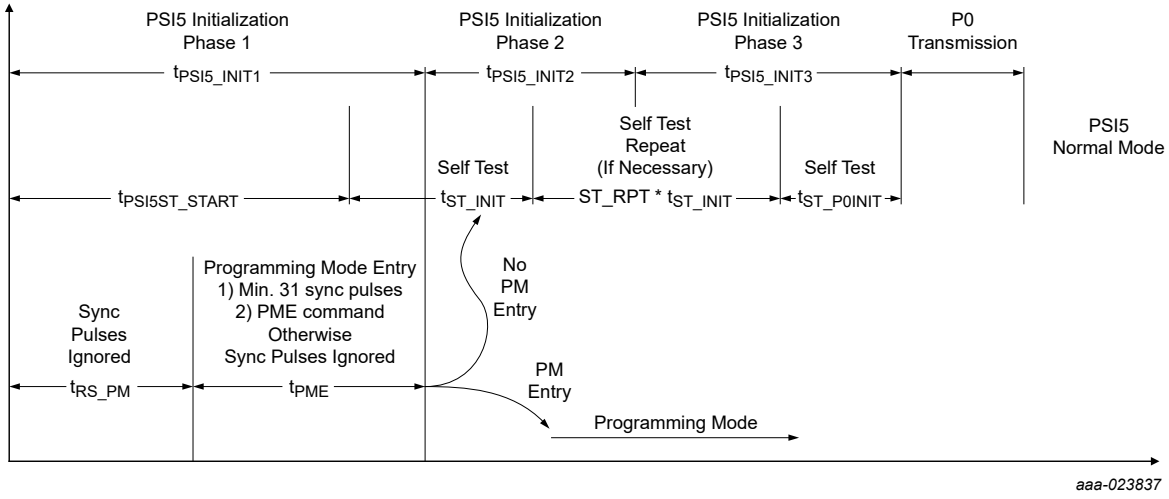


Figure 54. PSI5 initialization timing, synchronous mode

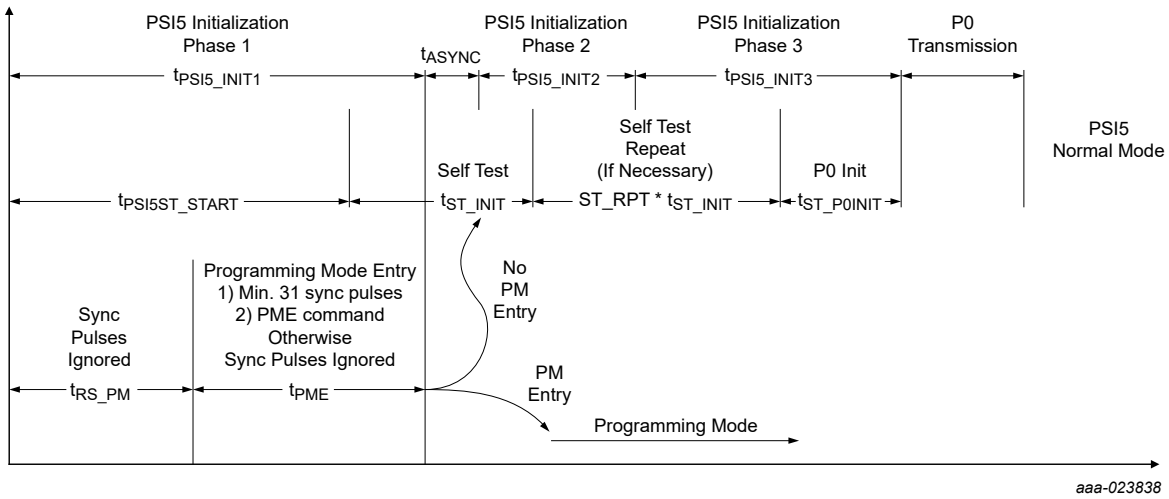


Figure 55. PSI5 initialization timing, asynchronous mode

11.3.4.1 PSI5 initialization phase 1

During PSI5 initialization phase 1, the device begins internal initialization and self-checks, but transmits no data. Initialization begins with the sequence below, shown in Section 11.3.4 "Initialization":

- Internal delay to ensure that analog circuitry has stabilized (t_{POR_PSI5})
- P0 filter initialization begins (t_{PSI5ST_START})
- Monitor for the programming mode entry sequence (t_{PME})
- If the programming mode entry sequence is not detected, the device enters initialization phase 2 (t_{PSI5_INIT2})

11.3.4.2 PSI5 initialization phase 2

During PSI5 initialization phase 2, the device continues its internal self-checks and transmits the PSI5 initialization phase 2 data. Initialization data is transmitted using the initialization data codes and IDs specified in Section 11.3.3.4 "PSI5 data field and data range values", and in the order shown in Section 11.3.4.2 "PSI5 initialization phase 2".

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Table 157. PSI5 initialization phase 2 data transmission order

D1							D2							...	D32						
$ID1_1$	$D1_1$	$ID1_2$	$D1_2$	...	$ID1_k$	$D1_k$	$ID2_1$	$D2_1$	$ID2_2$	$D2_2$	...	$ID2_k$	$D2_k$	...	$ID32_1$	$D32_1$	$ID32_2$	$D32_2$	...	$ID32_k$	$D32_k$
Repeat k times							Repeat k times							...	Repeat k times						

The initialization phase 2 time is calculated using Equation 14.

$$t_{Phase2} = Trans_{Nibble} \times k \times (DataFields) \times t_{S-S} \quad (14)$$

Where:

- $Trans_{Nibble}$ = # of transmissions per data nibble
- 2:1 for ID, and 1 for data
- k = The repetition rate for the data fields
- *DataFields* = 32 data fields or 48 data fields (if INIT2_EXT is set)
- t_{S-S} = Sync pulse period

11.3.4.2.1 PSI5 initialization phase 2 data transmissions

In PSI5 initialization phase 2, the device transmits a sequence of sensor specific configuration and serial number information. The transmission data is in conformance with the PSI5 specification[2], and AKLV29[3]. The data content and transmission format is shown in Table 158 and Table 159. Table 159 shows the phase 2 timing for different operating modes. Times are calculated using Equation 14 in Section 11.3.4.2 "PSI5 initialization phase 2".

Table 158. Initialization phase 2 time

Operating mode	Repetition rate (k)	# of transmissions	Nominal phase 2 time
Asynchronous mode (228 µs)	8	512	116.7 ms
Synchronous mode (500 µs)	4	256	128.0 ms

Table 159. PSI5 initialization phase 2 data

PSI5 V1.2 field ID #	PSI5 V1.2 nibble ID #	Page address	PSI5 nibble address	Register address	Description	Value
F1	D1	0	0000	USERDATA_0[3:0]	User-specific data	User
F2	D2, D3		0001, 0010	NA	Number of data blocks: 32: INIT2_EXT=0, 48: INIT2_EXT=1	0010 0000 or 0011 0000
F3	D4, D5		0011, 0100	USERDATA_1[3:0], USERDATA_1[7:4]	User-specific data	User
F4	D6, D7		0101, 0110	USERDATA_2[3:0], USERDATA_2[7:4]	User-specific data	User
F5	D8		0111	USERDATA_3[3:0]	User-specific data	User
	D9		1000	USERDATA_3[7:4]	User-specific data	User
F6	D10		1001	USERDATA_4[3:0]	User-specific data	User
	D11		1010	USERDATA_4[7:4]	User-specific data	User
F7	D12		1011	USERDATA_5[3:0]	User-specific data	User
	D13		1100	USERDATA_5[7:4]	User-specific data	User
	D14		1101	USERDATA_6[3:0]	User-specific data	User
F8	D15		1110	USERDATA_7[3:0]	User-specific data	User
	D16		1111	USERDATA_7[7:4]	User-specific data	User
	D17	1	0000	USERDATA_8[3:0]	User-specific data	User
	D18		0001	USERDATA_8[7:4]	User-specific data	User

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Table 159. PSI5 initialization phase 2 data*...continued*

PSI5 V1.2 field ID #	PSI5 V1.2 nibble ID #	Page address	PSI5 nibble address	Register address	Description	Value
F9	D19		0010	SN4[7:4]	Device serial number	Factory
	D20		0011	SN4[3:0]	Device serial number	Factory
	D21		0100	SN3[7:4]	Device serial number	Factory
	D22		0101	SN3[3:0]	Device serial number	Factory
	D23		0110	SN2[7:4]	Device serial number	Factory
	D24		0111	SN2[3:0]	Device serial number	Factory
	D25		1000	SN1[7:4]	Device serial number	Factory
	D26		1001	SN1[3:0]	Device serial number	Factory
	D27		1010	SN0[7:4]	Device serial number	Factory
	D28		1011	SN0[3:0]	Device serial number	Factory
	D29		1100	PN1[3:0]	Device Part Number	Factory
	D30		1101	PN0[7:4]	Device Part Number	Factory
	D31		1110	PN0[3:0]	Device Part Number	Factory
	D32		1111	USERDATA_6[7:4]	User-specific data	User
F10	D33	2	0000	Reserved	Reserved	Varies
	D34		0001	Reserved	Reserved	Varies
	D35		0010	Reserved	Reserved	Varies
	D36		0011	Reserved	Reserved	Varies
	D37		0100	Reserved	Reserved	Varies
	D38		0101	Reserved	Reserved	Varies
	D39		0110	Reserved	Reserved	Varies
	D40		0111	Reserved	Reserved	Varies
	D41		1000	Reserved	Reserved	Varies
	D42		1001	Reserved	Reserved	Varies
	D43		1010	Reserved	Reserved	Varies
	D44		1011	Reserved	Reserved	Varies
	D45		1100	Reserved	Reserved	Varies
	D46		1101	Reserved	Reserved	Varies
	D47		1110	Reserved	Reserved	Varies
	D48		1111	Reserved	Reserved	Varies

Note: *Constant values are transmitted for all fields marked as reserved.*

11.3.4.3 Internal self-test

Once initialization phase 1 completes, the device begins its internal self-test as described in Section 6.6.2 "Self-test functions".

11.3.4.4 Initialization phase 3

During PSI5 initialization phase 3, the device completes its internal self-checks, and transmits a combination of sensor busy or sensor ready messages as defined in Table 156. The number of sensor busy messages transmitted in initialization phase 3 varies depending on the mode of operation, and the number of self-test repetitions. Self-test is repeated on failure up to ST_RPT times to provide immunity to misuse inputs during initialization. Self-test terminates successfully after one successful self-test sequence.

Once internal self-test is completed, the device transmits two sensor ready commands.

After the sensor ready messages are transmitted, the device transmits the P0 absolute pressure value using the initialization codes shown in Section 11.3.3.4 "PSI5 data field and data range values". The P0 data to be transmitted is latched at the end of the transmission of the second sensor ready message. The initialization phase 3 response transmissions are listed here:

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- P0 transmission #0:

0	0	P0, D11	P0, D10	P0, D9

- P0 transmission #1:

0	1	P0, D8	P0, D7	P0, D6

- P0 transmission #2:

1	0	P0, D5	P0, D4	P0, D3

- P0 transmission #3:

1	1	P0, D2	P0, D1	P0, D0

In all modes, the ENDINIT bit is automatically set when the device exits initialization phase 3.

11.3.5 Normal mode

11.3.5.1 Asynchronous mode

The device can be programmed to respond in asynchronous mode as specified in Section 6.2.17 "PDCM_RSPSTx_x – DSI3 and PSI5 start time registers (address $26 to $29)".

In asynchronous mode, the device transmits data at a fixed rate (t_{ASYNC}) and will not respond to normal sync pulses. However, during initialization phase 1, the device will monitor sync pulses to decode the programming mode entry command and allow entry into programming mode.

11.3.5.2 Simultaneous sampling mode

The device can be programmed to respond in simultaneous sampling mode by programming the SS_EN bit to simultaneous sampling mode.

In simultaneous sampling mode, the most recent interpolated sensor data sample is latched at t_{TRIG} (rising edge of sync pulse) and transmitted starting at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG}.

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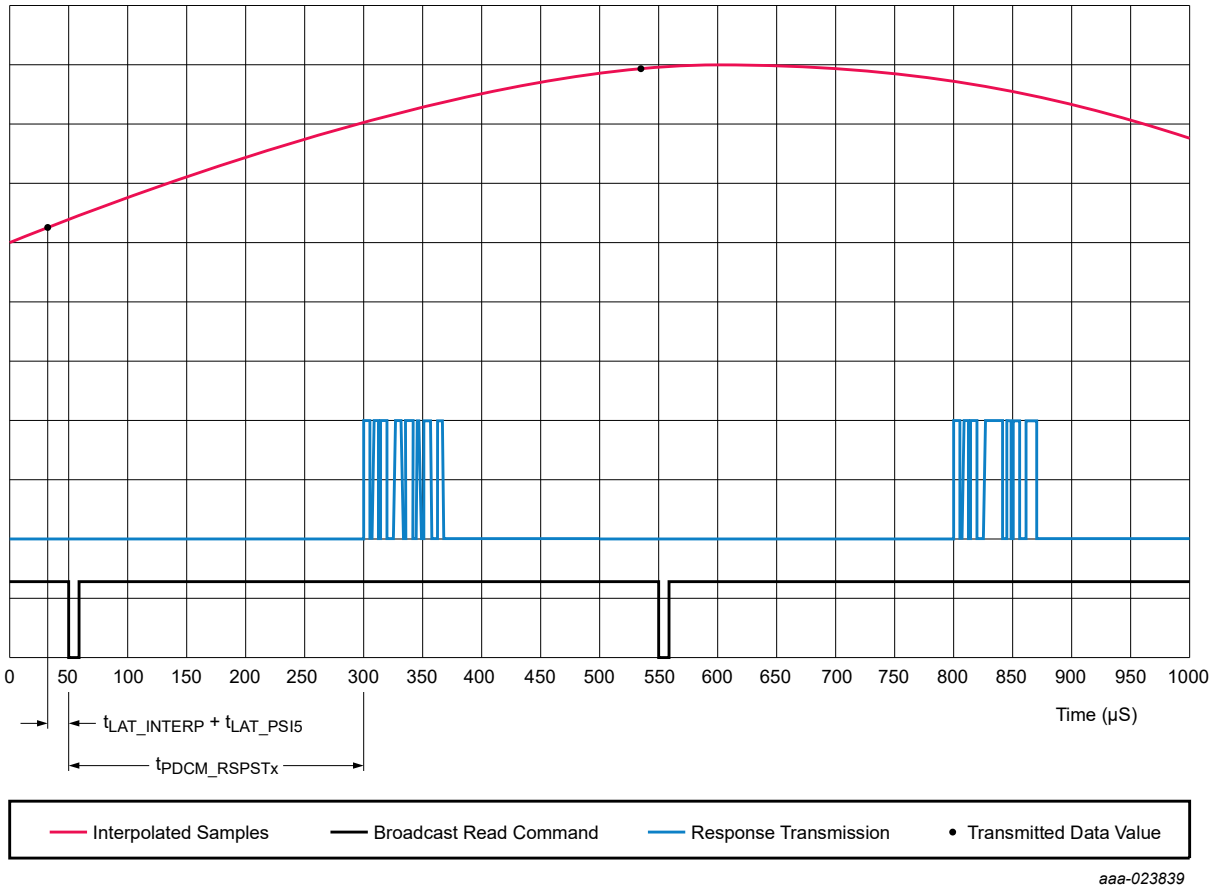


Figure 56. Simultaneous sampling mode

11.3.5.3 Synchronous sampling mode with minimum latency

The device can be programmed to respond in synchronous sampling mode with minimum latency by programming the SS_EN bit to synchronous sampling mode.

In synchronous sampling mode, the most recent interpolated sensor data sample is latched at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG} (rising edge of sync pulse). The data is transmitted starting at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG}.

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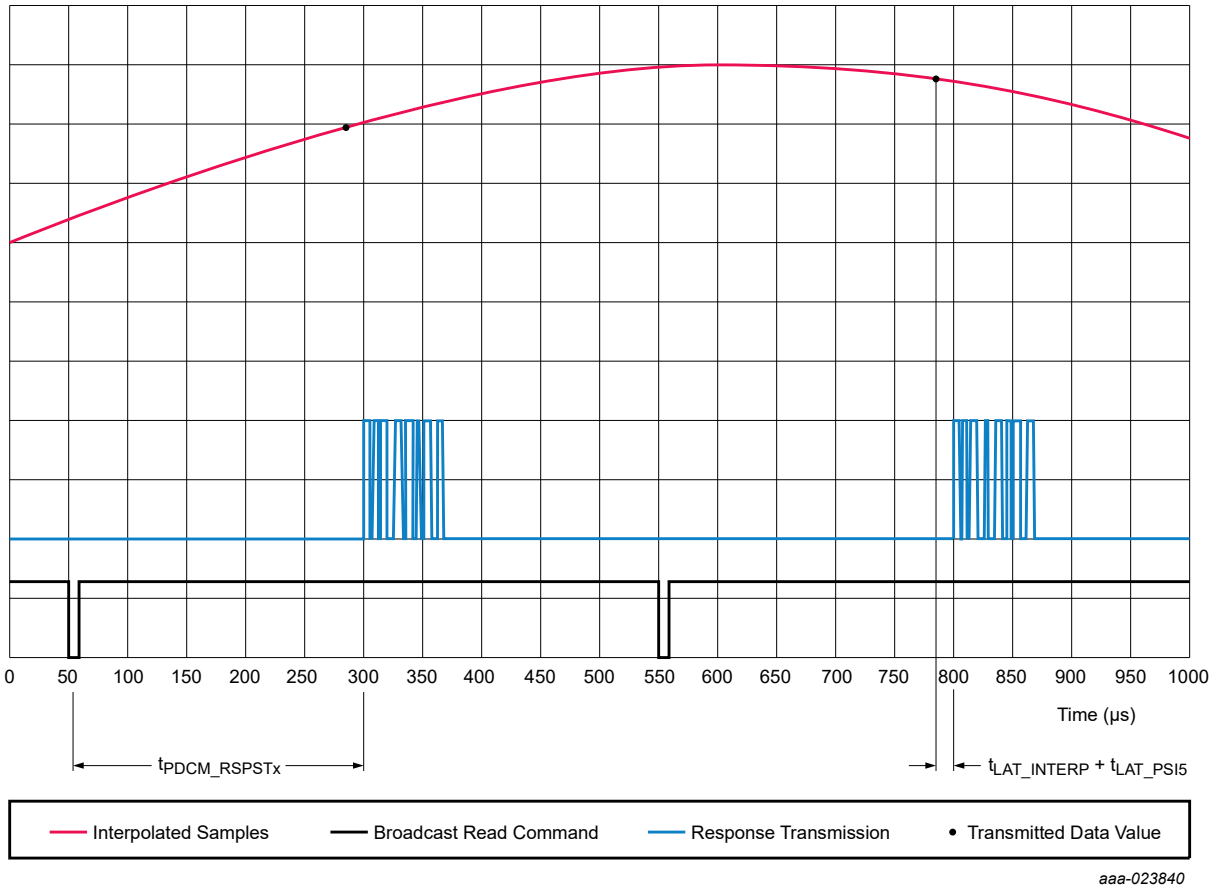


Figure 57. Synchronous sampling mode with minimum latency

11.3.6 Daisy chain mode

The device can be programmed to operate in daisy chain mode by setting the DAISY_CHAIN bit in the PSI5_CFG register. Daisy chain mode can be programmed to operate in either simultaneous sampling mode, or synchronous sampling mode by setting the SS_EN bit to the desired operating mode. In simultaneous sampling mode, the most recent interpolated sensor data sample is latched at t_{TRIG} (rising edge of sync pulse). In synchronous sampling mode, the most recent interpolated sensor data sample is latched at the time programmed in the PDCM_RSPSTx registers, relative to t_{TRIG} (rising edge of sync pulse).

When programmed to operate in daisy chain mode, the device follow this procedure:

- After a power on delay of t_{RS_PM}, the device waits for a PSI5 set address command defined in Table 161 and Table 162.
  - The set address command must be preceded by at least 31 consecutive sync pulses. All other commands must be preceded by either 31 consecutive sync pulses or five consecutive missing sync pulses.
  - The daisy chain programming command and response formats are defined in Section 11.3.8.2 "PSI5 programming mode – data link layer" using a sync pulse period of $t_{s\text{-}s_DC}$. The response settings are defined in Table 162, with the exception of the time slot.
  - The response to the PSI5 set address command and all other valid commands uses the address-based time slot specified in Table 163.
  - If a framing error or CRC error is detected on a received command, the device does not respond.

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- After receiving a valid address and completing the response, the device will decode and respond to all Table 163 commands sent to the sensor address it is set to. All responses will be transmitted in the address-based time slot specified in Table 163.
- When the run mode command is received, the device responds to the command using the address-based time slot(s) specified in Table 163. The device then ignores all commands and proceeds through initialization phase 2 and initialization phase 3 in response to sync pulses. The following response format is used, regardless of the state of the relevant bits in the device configuration registers:

Table 160. Frame parameter to reference

Parameter	Reference	Value
Time Slot	Section 6.2.17 "PDCM_RSPSTx_x – DSI3 and PSI5 start time registers (address $26 to $29)"	Address-based time slot specified in Table 163
Data Size	Section 6.2.12 "SOURCEID_x – source identification registers (address $1A, $1B)"	Data size controlled by the PDCMFORMAT bits
Error Checking	Section 6.2.16 "PSI5_CFG – PSI5 configuration register (address $25)"	Even parity
Baud Rate	Section 6.2.14 "CHIPTIME – chip time and bit time register (address $23)"	Baud rate controlled by the CHIPTIME bits

- Upon completion of initialization phase 3, the ENDINIT bit is set, the device enters normal mode and responds to all sync pulses with sensor data using the format above.

Table 161. Daisy chain programming commands and responses

CMD Type	SAdr			FC			Command	Response (OK)	
	A2	A1	A0	F2	F1	F0		RC	RD1
Short	0	0	0	A2	A1	A0	Set sensor address (daisy chain)	OK	SAdr
Short	1	1	1	0	0	0	Broadcast message – run mode	OK	000h
Short	SAdr <> 1 SAdr <> 6			0	0	0	Activate low-side bus switch BUSSW_CTRL[1:0] = '11	OK	000h
Short	SAdr <> 1 SAdr <> 6			1	1	1	Activate high-side bus switch BUSSW_CTRL[1:0] = '10'	OK	111h
Short	SAdr <> 1 SAdr <> 6			A2	A1	A0	Set sensor address (daisy chain)	OK	SAdr

Table 162. Daisy chain programming response code definitions

Response code	Definition	Value
RC = OK	Command message received properly	1E1h
RC = Error	Error during transmission of command message	1E2h
SAdr	Programmed sensor address, prepended with 0 s	Varies

Table 163. Valid daisy chain addresses

Sensor address (SAdr)			Description	Default time slot
A2	A1	A0		
0	0	0	Unprogrammed sensor	N/A
0	0	1	Sensor address 1	$t_{TIMESLOT_DC0}$
0	1	0	Sensor address 2	$t_{TIMESLOT_DC1_L}$
0	1	1	Sensor address 3	$t_{TIMESLOT_DC2_L}$
1	0	0	Sensor address 4	$t_{TIMESLOT_DC1_H}$
1	0	1	Sensor address 5	$t_{TIMESLOT_DC2_H}$
1	1	0	Sensor address 6	$t_{TIMESLOT_DC3_H}$
1	1	1	N/A	N/A

Note:

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- *Writes to sensor address 7 are ignored.*
- *If a successful programming mode entry command is received prior to a set address, daisy chain mode is disabled.*

11.3.7 Error handling

11.3.7.1 Daisy chain error handling

Table 164 shows the effect of internal failure modes on the daisy chain initialization procedure.

Table 164. Daisy chain error handling

Error condition	Effect on daisy chain
Supply error	Daisy chain commands Ignored. The device will not participate in daisy chain
Communication error	No effect. The device will participate in daisy chain as programmed.
Test mode enabled	Daisy chain commands ignored. The device will not participate in daisy chain
PABS out of range and/or mismatch error	No effect. The device will participate in daisy chain as programmed.
Temperature error	No effect. The device will participate in daisy chain as programmed.
Memory error	No effect. The device will participate in daisy chain as programmed.
Self-test error	No effect. The device will participate in daisy chain as programmed.
Device not locked	No effect. The device will participate in daisy chain as programmed.

11.3.7.2 Initialization phase 2 error handling

Table 165 shows the effect of internal failure modes on the initialization phase 2 transmissions. Some errors occurring in initialization phase 2 will prevent entry into initialization phase 3. Once the error is no longer present, the device will complete initialization phase 2 as necessary and then transition to initialization phase 3.

Table 165. Initialization phase 2 error handling

Error condition	Effect on initialization phase 2
Supply error	Temporary, sync pulses ignored
Communication error	No effect
Test mode enabled	No effect
PABS out of range and/or mismatch error	No effect
Temperature error	No effect. The device will attempt to transmit initialization phase 2 data.
Memory error	No effect. The device will attempt to transmit initialization phase 2 data.
Self-test error	No effect
Device not locked	No effect

11.3.7.3 Initialization phase 3 error handling

Table 166 shows the effect of internal failure modes on initialization procedures. Some errors occurring in initialization phase 3 will prevent entry into run mode until the error is no longer present. Once the error is no longer present, one or more sensor ready commands will be transmitted before entering run mode.

Table 166. Initialization phase 3 error handling

Error condition	Effect on initialization phase 3
Supply error	Temporary, sync pulses Ignored
Communication error	No effect
Test mode enabled	No effect
PABS out of range and/or mismatch error	No effect

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Table 166. Initialization phase 3 error handling...*continued*

Error condition	Effect on initialization phase 3
Temperature error	No effect. The device will attempt to transmit initialization phase 3 data.
Memory error	No effect. The device will attempt to transmit initialization phase 3 data.
Self-test error	No effect
Device not locked	Sensor ready replaced with sensor ready, but not locked transmission (UF2 region is unprogrammed)

11.3.7.4 Normal mode error handling

11.3.7.4.1 Standard error reporting

Table 167 summarizes the error reporting in normal mode if the PSI5 error extension option is disabled. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

Table 167. Standard error reporting

Error condition	Error code	Error priority	Error response
Supply error	NA		Temporary (normal transmissions continue once condition is removed)
Communication error	1EFh	6	
Test mode enabled	1EEh	2	
PABS out of range error	1EDh	5	
Temperature error	1ECh	4	
Memory error	1EBh	3	Latched until reset
Self-test error	1EAh	1	Latched until reset
Device not locked	NA		NA

11.3.7.4.2 PSI5 error extension option

If the PSI5 error extension option is enabled, additional error reporting is available as shown in Table 168. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

Table 168. PSI5 error extension option

Error condition	Error code	Error priority	Error response
Supply error	NA		Temporary (normal transmissions continue once condition is removed)
Communication error	1EFh	6	
Test mode enabled	1EEh	2	
PABS out of range error	1EDh	5	
Temperature error	1ECh	4	
Memory error	1EBh	3	Latched until reset
Self-test error	1EAh	1	Latched until reset
Device not locked	NA		NA

11.3.8 PSI5 diagnostic and programming mode

PSI5 programming mode is a synchronous communication mode that allows for bidirectional communication with the device. Programming mode is intended for factory programming of the OTP array and reading of diagnostic information. It is not intended for use in normal operation.

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11.3.8.1 PSI5 programming mode entry

The device enters programming mode if and only if the following sequence occurs:

- At least 31 sync pulses are detected, directly preceding the programming mode entry short command during the programming mode entry window shown in Section 11.3.4 "Initialization".
  - The window timing is defined in Section 10 "Dynamic characteristics" (t_{PME}).
  - The sync pulses and programming mode entry command must be received with a sync pulse period of t_{S-S_PM}

If the programming mode entry requirement is not met:

- Programming mode entry is blocked until the device is reset.
- The device proceeds with PSI5 initialization phase 2 and PSI5 initialization phase 3.
- The device enters normal mode, and responds as programmed to normal sync pulses.

If the programming mode entry requirement is met:

- Normal transmissions to sync pulses are terminated.
- The device will detect commands if the start condition is met as described in Section 11.3.8.2.2 "PSI5 programming mode – command message format".
- The device responds only to valid PSI5 short and XLong commands addressed to sensor address '001', as defined in Section 11.3.8.3 "PSI5 programming mode command and response summary".

11.3.8.2 PSI5 programming mode – data link layer

11.3.8.2.1 PSI5 programming mode – command bit encoding

Commands messages are transmitted via the modulation of the supply voltage. The presence of a sync pulse is a logic '1' and the absence of a sync pulse is a logic '0'. Sync pulses are expected at a rate of t_{S-S_PM}.

11.3.8.2.2 PSI5 programming mode – command message format

Command message data frames consist of a start condition, three start bits (S[2:0]), a 3-bit sensor address (SAdr[2:0]), a 3-bit function code (FC[2:0]), an optional register address (RAdr[7:0]), an optional data field (D[7:0]), and a 3-bit CRC (C[2:0]. The start condition consists of one of the following:

1. A minimum of five consecutive logic '0's (with no sync bits)
2. A minimum of 31 consecutive logic '1's (this includes logic '1's transmitted for the previous response)

The command message format is shown in Table 169.

Table 169. Programming mode via PSI5 command data format

Start bits			Sensor address			Function code			Register address								Data								CRC			Response		
S2	S1	S0	SA0	SA1	SA2	FC0	FC1	FC2	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	D0	D1	D2	D3	D4	D5	D6	D7	C2	C1	C0	RC	RD1	RD0
0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	$3FF	$3FF	$3FF
																									CRC					
																	Data to be written to register (optional)													
									Register Address (optional)																						
						Function codes (See Section 11.3.8.3 "PSI5 programming mode command and response summary")																										
			Sensor address – Fixed at 001																												
Start bit sequence = 010																														

Bit stuffing is necessary to maintain a synchronized timebase between the command master and the device. A logic '1' sync bit is added every 4th bit in the command message to ensure that there will never be more than three logic '0' bits in a row.

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Table 170. Programming mode via PSI5 XLong command data format with sync bits

Start bits				Sensor address				Function code				Register address										Data														CRC					Response		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0		RC	RD1	RD0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0		$1E2	$3FF	$3FF

Once a command is received and verified, the device expects two to three consecutive sync pulses (depending upon the command message lengths described below). There is no delay restriction between the command and the first sync pulse for the response. Once the first sync pulse for the response is received, each successive response sync pulse must be received within the programming mode sync pulse period specified ($t_{S\text{-}S_PM}$) or a framing error may occur.

For each of these sync pulses, The device will respond with the following settings:

Table 171. Programming mode via PSI5 response message settings

Parameter	Value
Time slot	$t_{TIMESLOT_DC0}$
Data size	10-bit data
Error checking	Even parity
Baud rate	125 kBd
Sync pulse pulldown	Disabled

11.3.8.2.3 Short frame command and response format

Short frames are the simplest type of command message. No data is transmitted in a short frame command. Only specific instructions are performed in response to short frame commands. The short frame format is shown in Table 172. Short frame commands and responses are defined in Section 11.3.8.3 "PSI5 programming mode command and response summary".

The device only supports a short command for programming mode entry.

Table 172. Programming mode via PSI5 short frame command and response format

Start bits				Sensor address				Function code				CRC				Response	
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	C2	C1	C0		RC	RD1
0	1	0	1	1	0	0	1	0	0	1	1	0	0	0		$1E2	$3FF

11.3.8.2.4 Long frame command and response format

Long frames allow for the transmission of data nibbles for register writes. The device can provide register data in response to a read or write request. The long frame format is shown in Table 173. Long frame commands and responses are defined in Section 11.3.8.3 "PSI5 programming mode command and response summary".

The device does not support the long frame command.

Table 173. Programming mode via PSI5 long frame command and response format

Start bits				Sensor address				Function code				Register address								Data					CRC					Response		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	D0	D1	D2	Sy	D3	C2	C1	Sy	C0		RC	RD1	RD0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	1	0		$1E2	$3FF	$3FF

11.3.8.2.5 Extra long frame command and response format

Extra long frames allow for the transmission of address and data bytes for register reads and writes. The device can provide register data in response to a read or write request. The extra long frame format is shown in Table 174. Extra long frame commands and responses are defined in Section 11.3.8.3 "PSI5 programming mode command and response summary".

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The device supports register read and register write extra long commands.

Table 174. Programming mode via PSI5 extra long command and response format

Start bits				Sensor address				Function code				Register address									Data												CRC					Response		
S2	S1	S0	Sy	SA(	SA1	SA2	Sy	FC(	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0		RC	RD1	RD0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0		S1E2	3FF	3FF

11.3.8.2.6 Command message CRC

Programming mode command error checking is accomplished by a 3-bit CRC. The 3-bit CRC is calculated using all message bits except start bits and sync bits. The CRC verification uses a generator polynomial of g(x) = x^3+x+1, with a nondirect seed value = '111'. The message data is provided to the CRC calculator in the order received (LSB first, SAdr, FC, RAdr, Data), and then augmented with three '0's. Table 155 shows examples of CRC calculation values for 10-bit data transmissions.

The calculated CRC is then compared against the received 3-bit CRC (received MSB first). If a CRC mismatch is detected, the device responds with a CRC Error response as defined in Section 11.3.8.4 "Programming mode via PSI5 error response summary".

11.3.8.2.7 Command sync pulse blanking time

In programming mode and programming mode entry, the device employs a fixed sync pulse blanking time of $t_{SYNC_OFF_250}$ regardless of the state of the PDCM_CMD_B register value.

11.3.8.2.8 Command timeout

In the event that the device does not detect a sync pulse within a 4-bit window time, the command reception will be terminated and the device will respond to the next sync pulse with a short frame framing error response as defined in Section 11.3.8.4 "Programming mode via PSI5 error response summary".

11.3.8.3 PSI5 programming mode command and response summary

Table 175. Programming mode via PSI5 commands and responses

CMD Type	SAdr	FC FC[2:0]	Command	Register address	Data Field	Response (OK)			Response (Error)		
						RC	RD1	RD0	RC	RD1	RD0
Short	001	100	Invalid command	N/A	N/A	No response			No response		
Short		101	Invalid command	N/A	N/A	No response			No response		
Short		110	Invalid command	N/A	N/A	No response			No response		
Short		111	Enter programming mode	N/A	N/A	OK	0CAh	N/A	No response		
Long		010	Invalid command	N/A	N/A	No response			No response		
Long		011	Invalid command	N/A	N/A	No response			No response		
XLong		000	Read register located at address RA7:RA0	Varies	Varies	OK	RData	RData+1	Error	ErrN	000h
XLong		001	Write WData to register RA7:RA0	Varies	Varies	OK	WData	RA7:RA0	Error	ErrN	000h

Table 176. Programming mode via PSI5 response code definitions

Response Code	Definition	Value
RC = OK	Command message received properly	1E1h
RC = Error	Error during transmission of command message	1E2h
RData	Byte contents of register located at address RA7:RA1 with RA0 = 0	Varies
RData + 1	Byte contents of register located at address RA7:RA1 with RA0 = 1	Varies
WData	Byte contents of register located at address RA7:RA0	Varies

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11.3.8.4 Programming mode via PSI5 error response summary

Table 177. Error response summary

ErrN	Mnemonic	Description	Supported
0000	General	General error	No
0001	Framing	Framing error (four consecutive zeroes)	Yes
0010	CRC	CRC error on received message	Yes
0011	Address	Sensor address not supported	No (Invalid address is ignored)
0100	FC	Function code not supported	No (N/A)
0101	Reserved	Reserved	No
0110			
0111			
1000	Reserved	Reserved	No
1001			
1010			
1011			
1100			
1101			
1110			
1111			

ErrN is transmitted in the four LSBs of RD1. All other bits in the response data field are set to '0'.

11.3.9 PSI5 OTP programming procedure

1. Enter programming mode.

2. Set $V_{CC} = V_{PP}$

3. Load desired data into the desired registers using PSI5 write commands.

4. Write the necessary OTP program sequence to the WRITE_OTP_EN register for the desired OTP region to be written.

5. Delay t_{PROG_TIME} after the completion of the write OTP program to allow for completion of the OTP writes.

6. To confirm that no errors occurred during the OTP writes, read the DEVSTAT1 register.

7. Read back the register values that were written and compare to the desired values to confirm successful OTP writes.

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11.4 DSI3 discovery mode

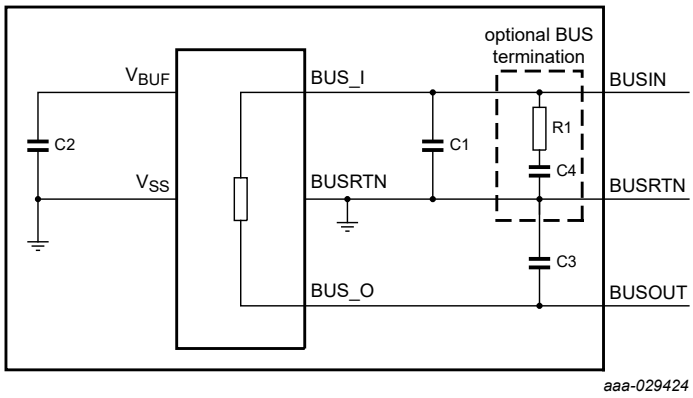


Figure 58. DSI3 discovery mode application diagram

Table 178. External component recommendations

Notes:

- *The total bus capacitance must not exceed the values specified in the DSI3 standard[1].*
- *The external components are dependent on the bus master and bus impedance and may vary from application to application.*

Ref	Type	Typical value description	Component value selection and range	Comment
R1	General purpose	330 Ω, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Optional bus termination for high inductance bus wire connections. For optimal EMC performance, this component along with C4 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C1	Ceramic	220 pF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing.	For optimal EMC performance, this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.	For optimal EMC performance, this component is to be placed as close to the V_{BUF} and BUSRTN pins as possible.
C3	Ceramic	100 pF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	For optimal EMC performance, this component is to be placed as close to the BUS_O and BUSRTN connector pins as possible.
C4	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Optional bus termination for high inductance bus wire connections. For optimal EMC performance, this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.

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11.5 DSI3 switch connected daisy chain mode

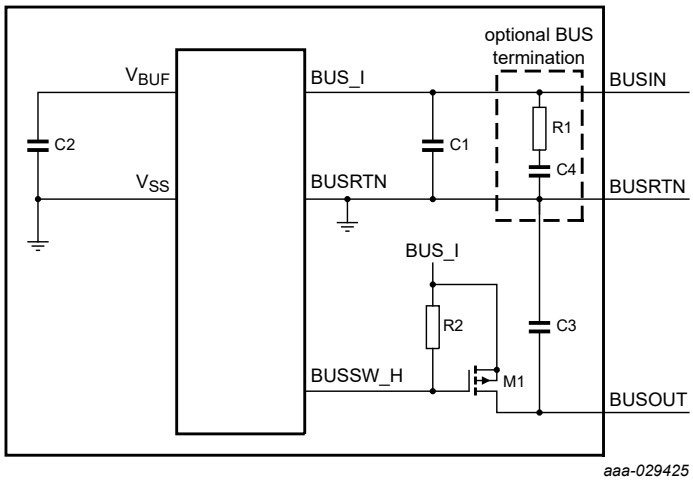


Figure 59. DSI3 switch connected daisy chain application diagram

Table 179. External component recommendations

Notes:

- *The total bus capacitance must not exceed the values specified in the DSI3 standard[1].*
- *The external components are dependent on the bus master and bus impedance and may vary from application to application.*

Ref	Type	Typical value description	Component value selection and range	Comment
R1	General purpose	330 Ω, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Optional bus termination for high inductance bus wire connections. For optimal EMC performance, this component along with C4 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
R2	General purpose	100 kΩ, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Pullup resistor for external high-side daisy chain FET
C1	Ceramic	220 pF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing.	For optimal EMC performance, this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.	For optimal EMC performance, this component is to be placed as close to the V_{BUF} and BUSRTN pins as possible.
C3	Ceramic	100 pF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	For optimal EMC performance, this component is to be placed as close to the BUS_O and BUSRTN connector pins as possible.
C4	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Optional bus termination for high inductance bus wire connections. For optimal EMC performance, this component along with R1 are to be placed as close to the BUS_I and BUSRTN connector pins as possible.
M1	P-channel MOSFET	NTR4502PT1G, or similar	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	High-side daisy chain transistor

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11.6 PSI5 parallel or universal mode

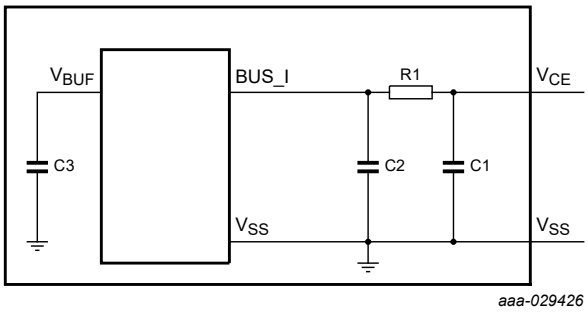


Figure 60. PSI5 parallel or universal mode application diagram

Table 180. External component recommendations

Notes:

- *The total bus capacitance must not exceed the values specified in the PSI5 standard[2].*
- *R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.*
- *If the high baud rate is used, it is recommended to reduce the value of C2. The actual value will depend on the bus configuration and number of slaves.*

Ref	Type	Typical value description	Component value selection and range	Comment
R1	General purpose	10 Ω, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. For proper device function, the minimum value can be 0 Ω. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 20.5 Ω. If the low response current is used, the maximum resistance including all tolerances is 33.3 Ω.	V_{CC} filtering and signal damping
C1	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	V_{CC} power supply decoupling and signal damping. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	15 nF, 10 %, 50 V minimum, X7R	—	V_{CC} power supply decoupling. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN pins as possible.
C3	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.	For optimal EMC performance, this component is to be placed as close to the V_{BUF} and BUSRTN pins as possible.

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11.7 PSI5 daisy chain mode

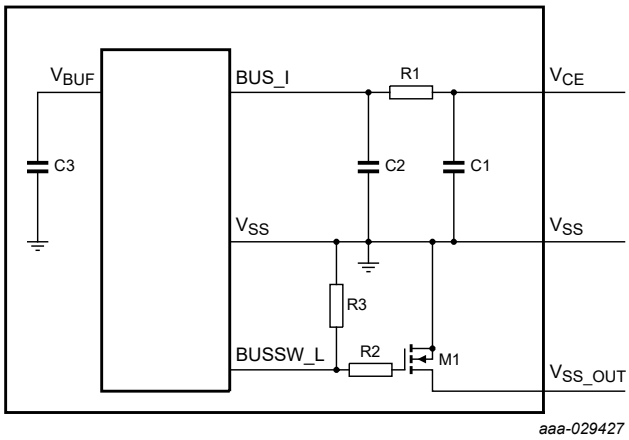


Figure 61. PSI5 daisy chain mode application diagram

Table 181. External component recommendations

Notes:

- *R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.*
- *If the high baud rate is used, it is recommended to reduce the value of C2. The actual value will depend on the bus configuration and number of slaves.*

Ref	Type	Typical value description	Component value selection and range	Comment
R1	General purpose	10 Ω, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. For proper device function, the minimum value can be 0 Ω. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 20.5 Ω. If the low response current is used, the maximum resistance including all tolerances is 33.3 Ω.	V_{CC} filtering and signal damping
R2	General purpose	20 kΩ, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Gate resistor for external low side daisy chain FET
R3	General purpose	100 kΩ, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Gate pulldown resistor for external low side daisy chain FET
C1	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	V_{CC} power supply decoupling and signal damping. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	15 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	V_{CC} power supply decoupling. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN pins as possible.
C3	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.	For optimal EMC performance, this component is to be placed as close to the V_{BUF} and BUSRTN pins as possible.
M1	N-channel MOSFET	NTR4501NT1G, or similar	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Low-side daisy chain transistor

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12 Package information

Consult the most recently issued drawing before initiating or completing a design. The drawings are available for download at https://www.nxp.com/docs/en/package-information/SOT1573-2(SC).pdf .

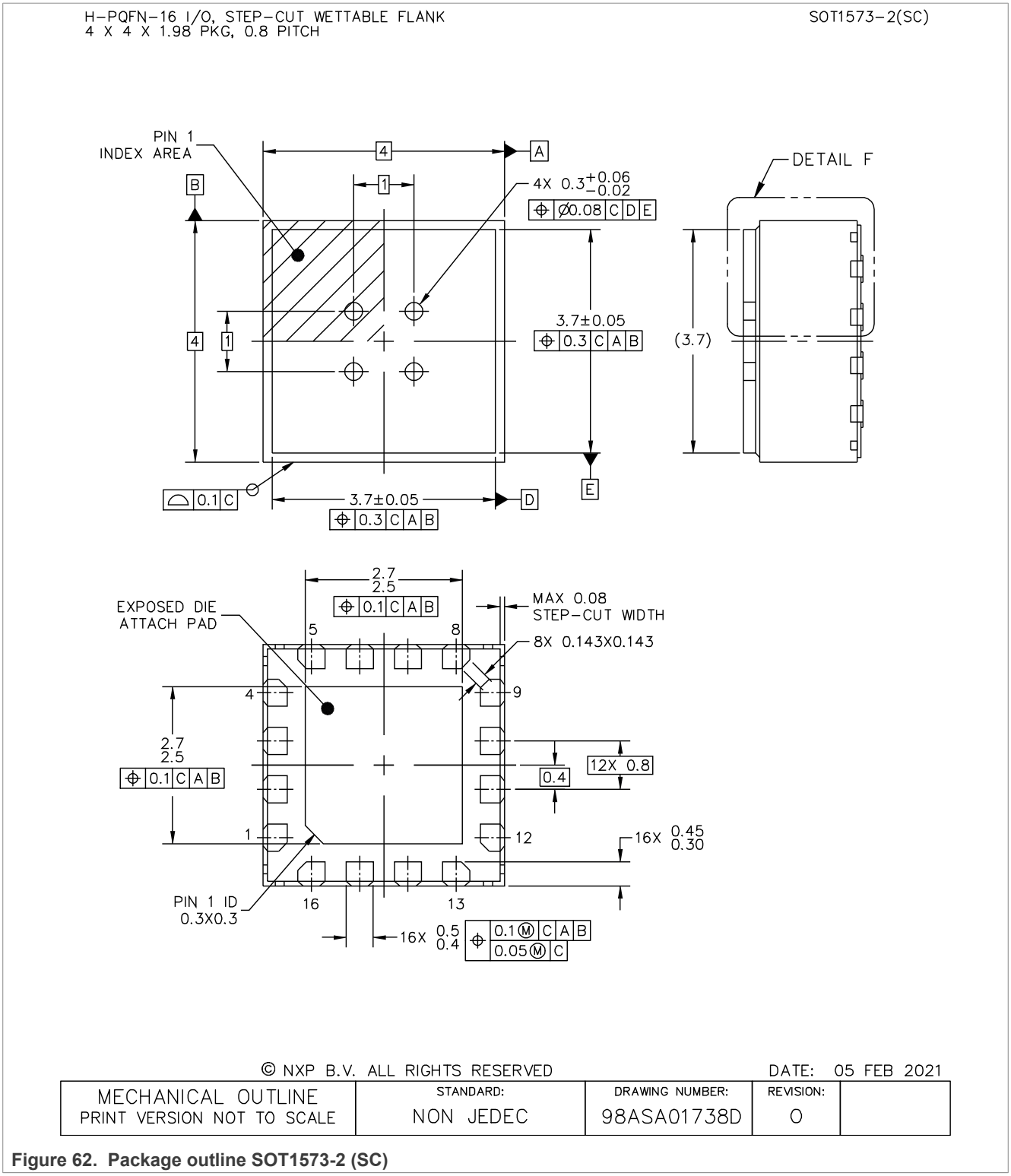


Figure 62. Package outline SOT1573-2 (SC)

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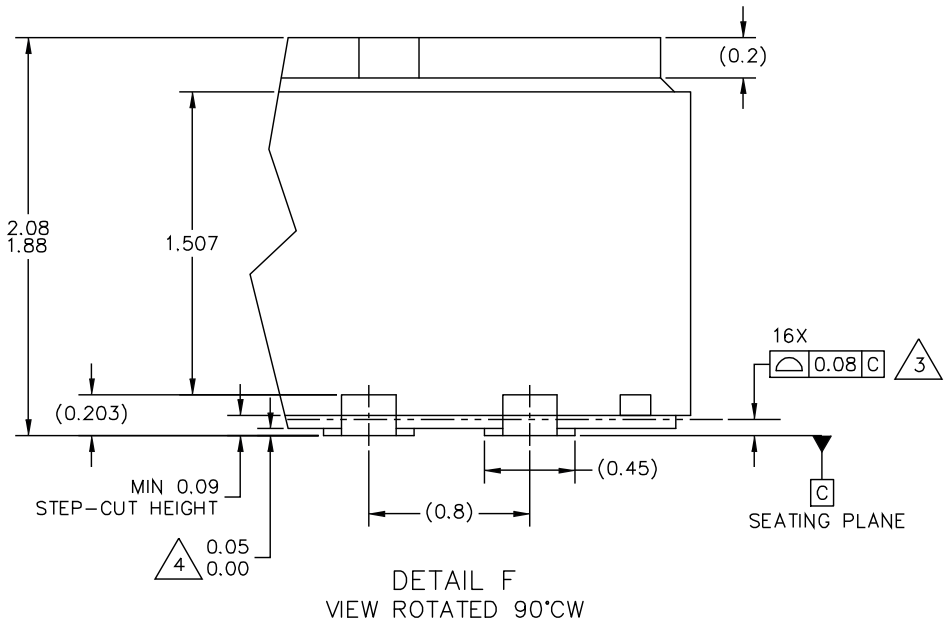
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Table 182. SOT1573-2(SC) hole dimensions

Lid parameter	POR lid	New lid
# of holes	1	4
Hole diameter (mm)	0.5	0.3
Air hole upper tolerance (mm)	0.05	0.06
Air hole lower tolerance (mm)	0.02	0.02
Lid radius angle (mm)	0.25	0.25
Material hardness	H	½ H

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DATE: 05 FEB 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01738D	REVISION: O	

Figure 63. Package outline detail HQFN (SOT1573-2(SC))

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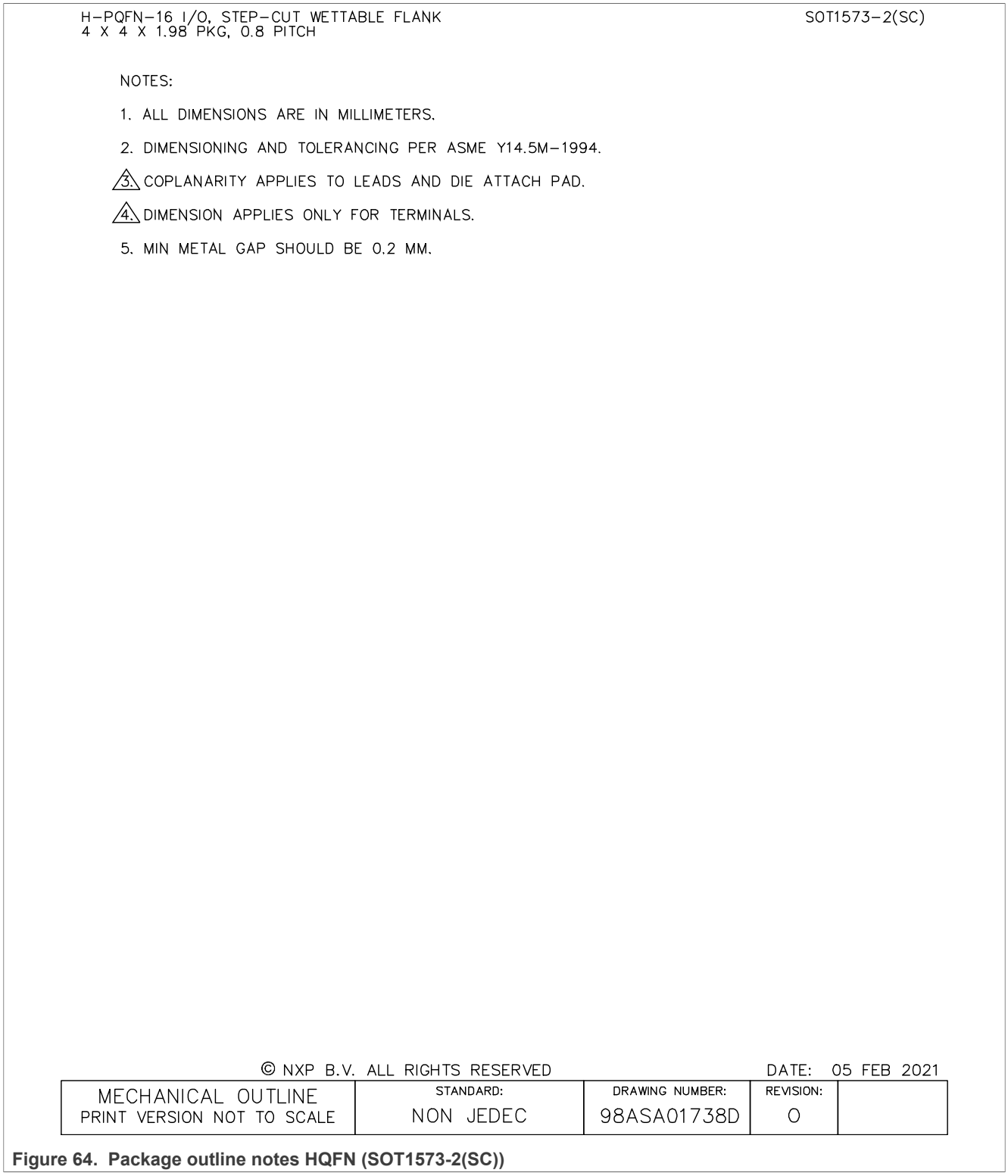


Figure 64. Package outline notes HQFN (SOT1573-2(SC))

12.1 Footprint

Reference NXP application note[6] AN1902 for the latest revision.

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13 Soldering

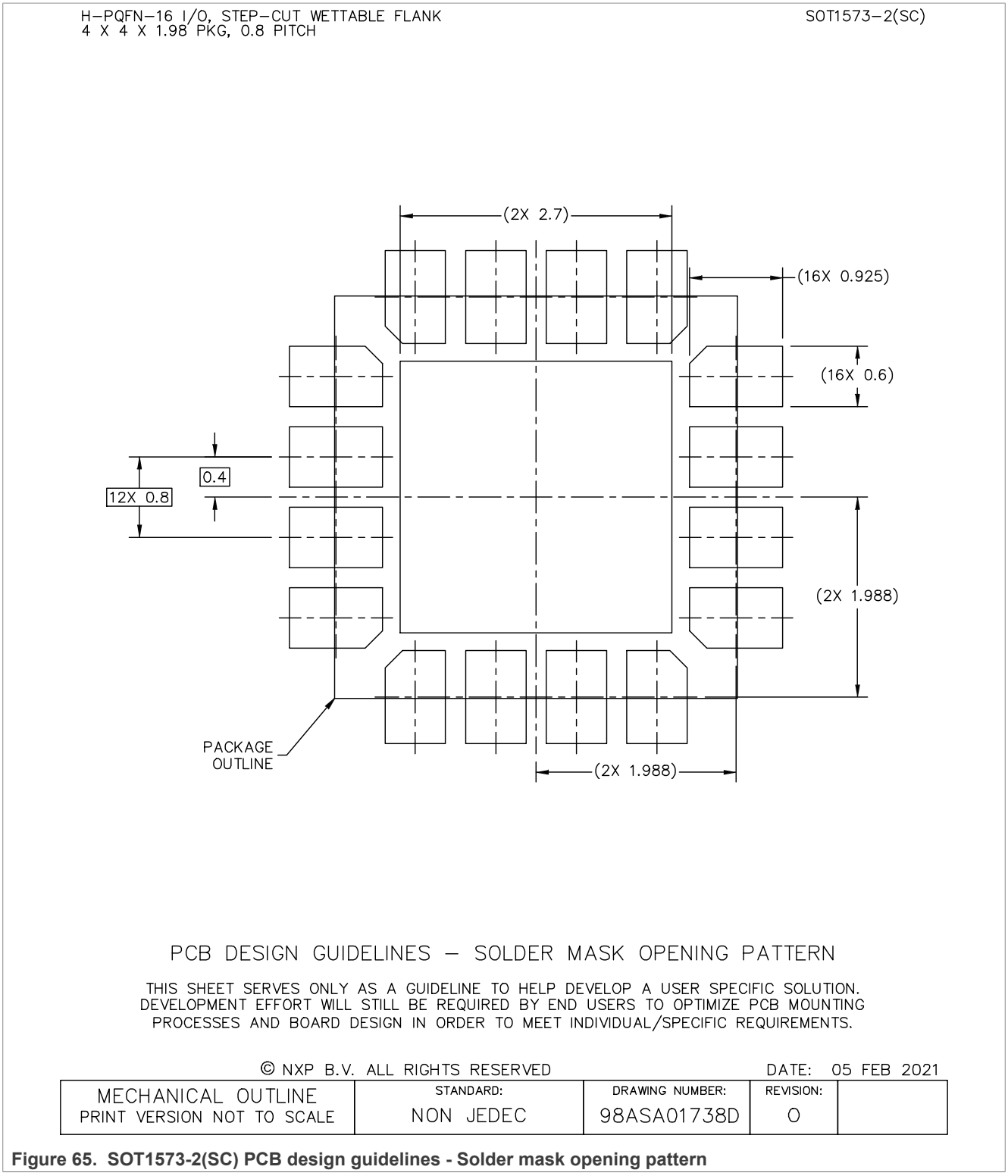


Figure 65. SOT1573-2(SC) PCB design guidelines - Solder mask opening pattern

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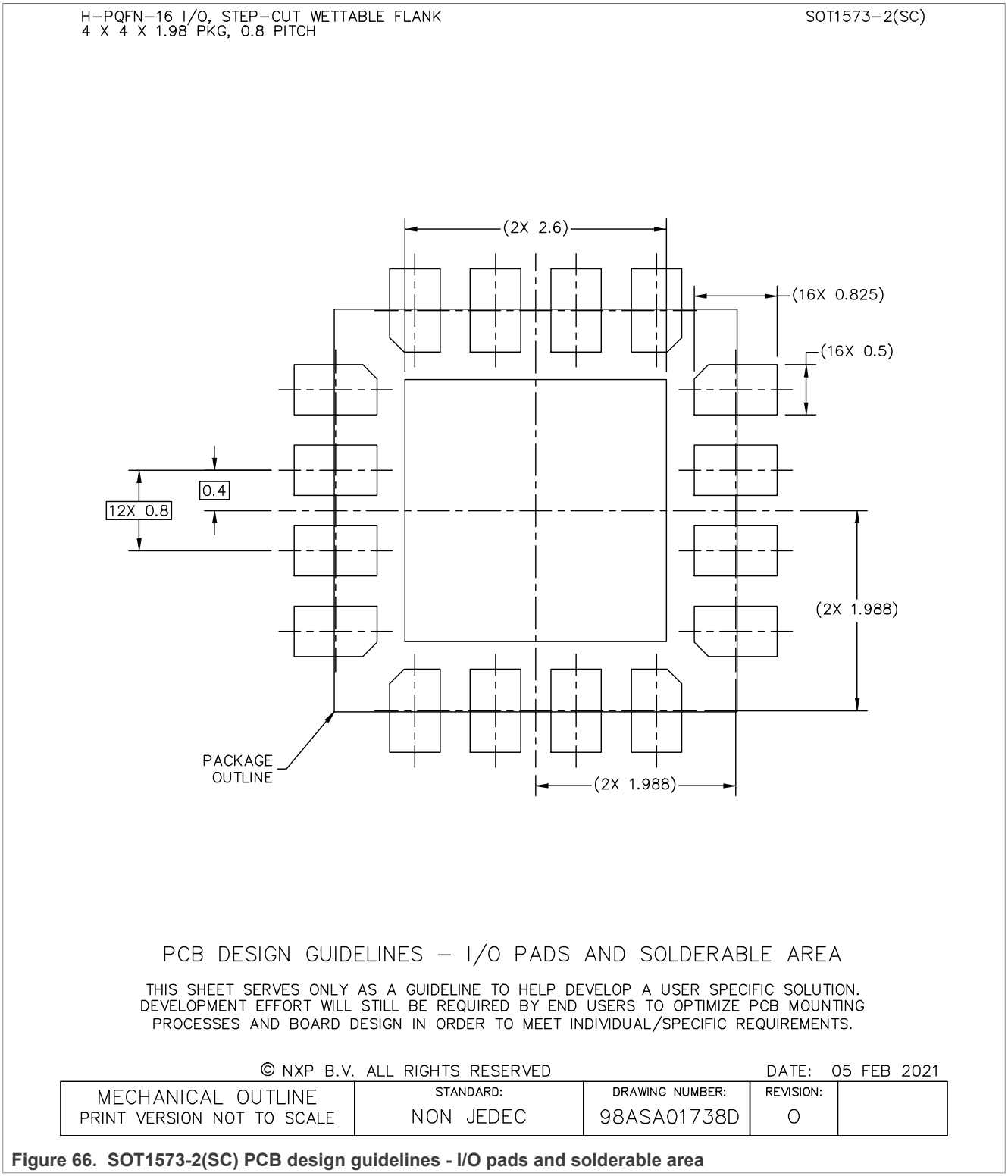


Figure 66. SOT1573-2(SC) PCB design guidelines - I/O pads and solderable area

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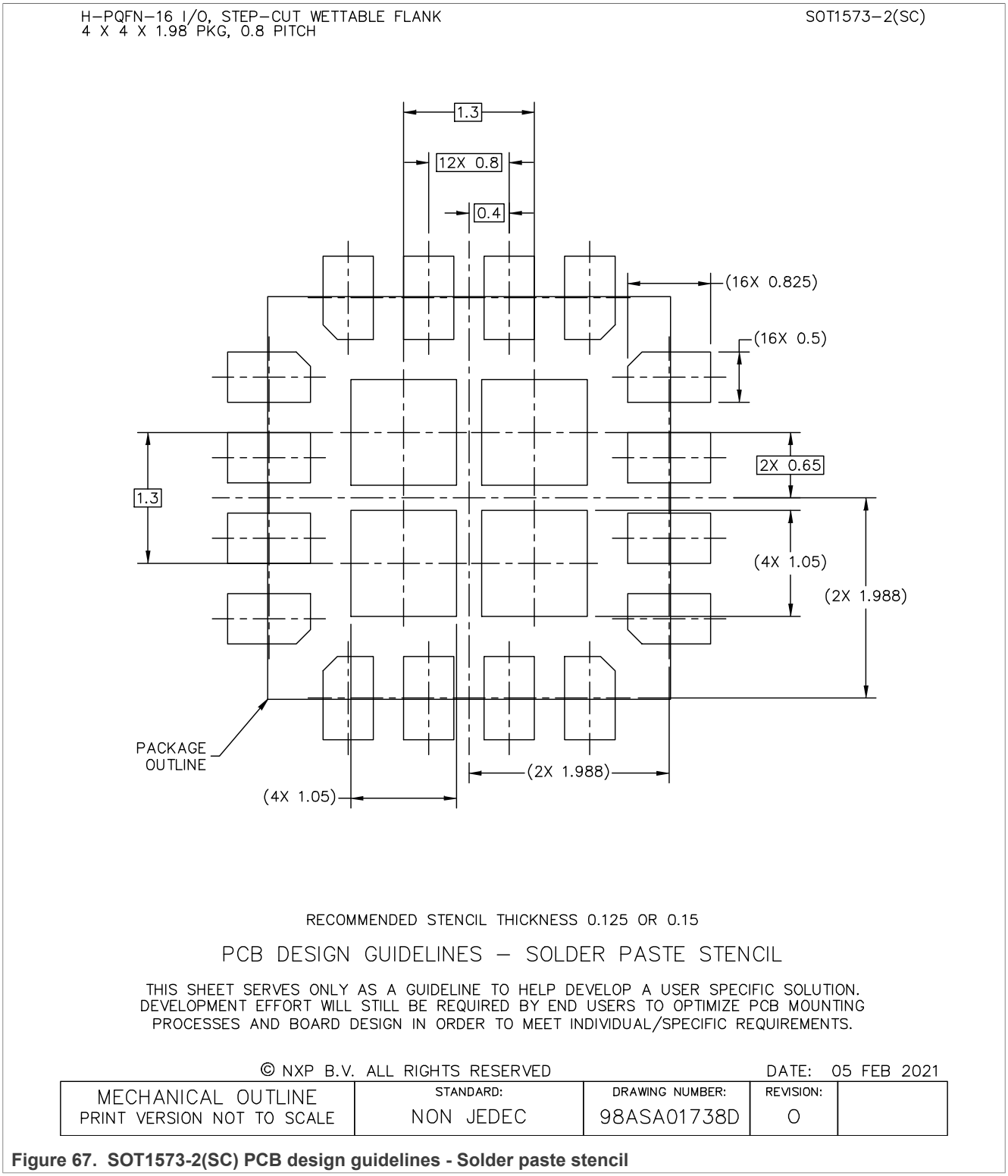


Figure 67. SOT1573-2(SC) PCB design guidelines - Solder paste stencil

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14 Mounting recommendations

The package should be mounted with the pressure port pointing away from sources of debris which might otherwise plug the sensor.

A plugged port exhibits no change in pressure and can be cross checked in the user software.

Refer to NXP application note AN1902[6] for proper printed circuit board attributes and recommendations.

15 References

[1] DSI3 Standard Revision 1.0, Dated February 16, 2011

[2] PSI5 Technical Specification version 2.1, dated October 8, 2012

[3] AKLV29 V1.30

[4] AEC-Q100, Revision G, AEC-Q006

[5] ISO16750, Environmental conditions, and testing for electrical and electronic equipment — Parts 1, 3, 4 and 5

[6] AN1902, Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages https://www.nxp.com/docs/en/application-note/AN1902.pdf

16 Revision history

Table 183. Revision history

Document ID	Release date	Data sheet status	Change notice	Supercedes
FXPS71407 v.3.4	20231129	Product data sheet	—	FXPS71407 v.3.3
Modifications:	• Section 3.1, Table 2, removed footnote 3 following "FXPS7140P7". The default protocol DSI3 does not apply to this PSI5 part.			
FXPS71407 v.3.3	20231005	Product data sheet	—	FXPS71407 v.3.2
FXPS71407 v.3.2	20221205	Product data sheet	—	FXPS71407 v.3.1
FXPS71407 v.3.1	20211208	Product data sheet	—	FXPS71407 v.3
FXPS71407 v.3	20211119	Product data sheet	—	FXPS71406 v.2
FXPS71406 v.2	20210805	Preliminary	—	FXPS71406 v.1
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