ESP32-C61-WROOM-1
ESP32-C61-WROOM-1U

Datasheet Version1.1

Module that supports 2.4 GHz Wi-Fi 6 (802.11ax), Bluetooth® 5 (LE)
Built around ESP32-C61 series of SoCs, 32-bit RISC-V single-core microprocessor
Flash up to 16 MB, PSRAM up to 8 MB
Up to 23 GPIOs, rich set of peripherals
On-board PCB antenna or external antenna connector

ESP32-C61-WROOM-1

ESP32-C61-WROOM-1U

ESPRESSIF

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/documentation/esp32-c61-wroom-1_wroom-1u_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-C61 series of SoCs embedded, 32-bit RISC-V single-core microprocessor, up to 160 MHz
- ROM: 256 KB
- SRAM: 320 KB
- Up to 8 MB PSRAM

Wi-Fi

- 1T1R in 2.4 GHz band
- Operating frequency: 2412 ~ 2484 MHz
- IEEE 802.11ax-compliant
  - 20 MHz-only non-AP mode
  - MCS0 ~ MCS9
  - Uplink and downlink OFDMA to enhance connectivity and performance in congested environments for IoT applications
  - Downlink MU-MIMO (multi-user, multiple input, multiple output) to increase network capacity
  - Beamformee that improves signal quality
  - Spatial reuse to maximize parallel transmissions
  - Target wake time (TWT) that optimizes power saving mechanisms
- Fully compatible with IEEE 802.11b/g/n protocol
  - 20 MHz and 40 MHz bandwidth
  - Data rate up to 150 Mbps
  - Wi-Fi Multimedia (WMM)
  - TX/RX A-MPDU, TX/RX A-MSDU
  - Immediate Block ACK
  - Fragmentation and defragmentation
  - Transmission opportunity (TXOP)
  - Automatic Beacon monitoring (hardware TSF)
  - Four virtual Wi-Fi interfaces
  - Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
    Note that when ESP32-C61 scans in Station mode, the SoftAP channel will change along with the Station channel
  - 802.11mc FTM

Bluetooth®

- Bluetooth LE
- Bluetooth mesh
- High power mode (20 dBm)
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- LE power control
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- GPIO, SPI, UART, I2C, I2S, LED PWM, USB Serial/JTAG controller, GDMA, On-chip debug functionality via JTAG, event task matrix, ADC, temperature sensor, brown-out detector, analog voltage comparator, general-purpose timers, system timer, and watchdog timers

Integrated Components on Module

- 40 MHz crystal oscillator
- Quad SPI flash

Antenna Options

- ESP32-C61-WROOM-1: On-board PCB antenna
- ESP32-C61-WROOM-1U: External antenna via a connector

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature:
  - 85 °C version module: −40 ~ 85 °C
  - 105 °C version module: −40 ~ 105 °C

1.2 Series Comparison

ESP32-C61-WROOM-1 and ESP32-C61-WROOM-1U are two powerful, general-purpose Wi-Fi, and Bluetooth LE modules. The rich set of peripherals and high performance make the module an ideal choice for smart homes, industrial automation, health care, consumer electronics, etc.

ESP32-C61-WROOM-1 comes with a PCB antenna. ESP32-C61-WROOM-1U comes with a connector for an external antenna. The information in this datasheet is applicable to both modules.

A wide selection of module variants are available. The variant nomenclature is shown in Figure 1, and the series comparisons are listed in Table 1 and Table 2.

The nomenclature for the module variants is as follows:

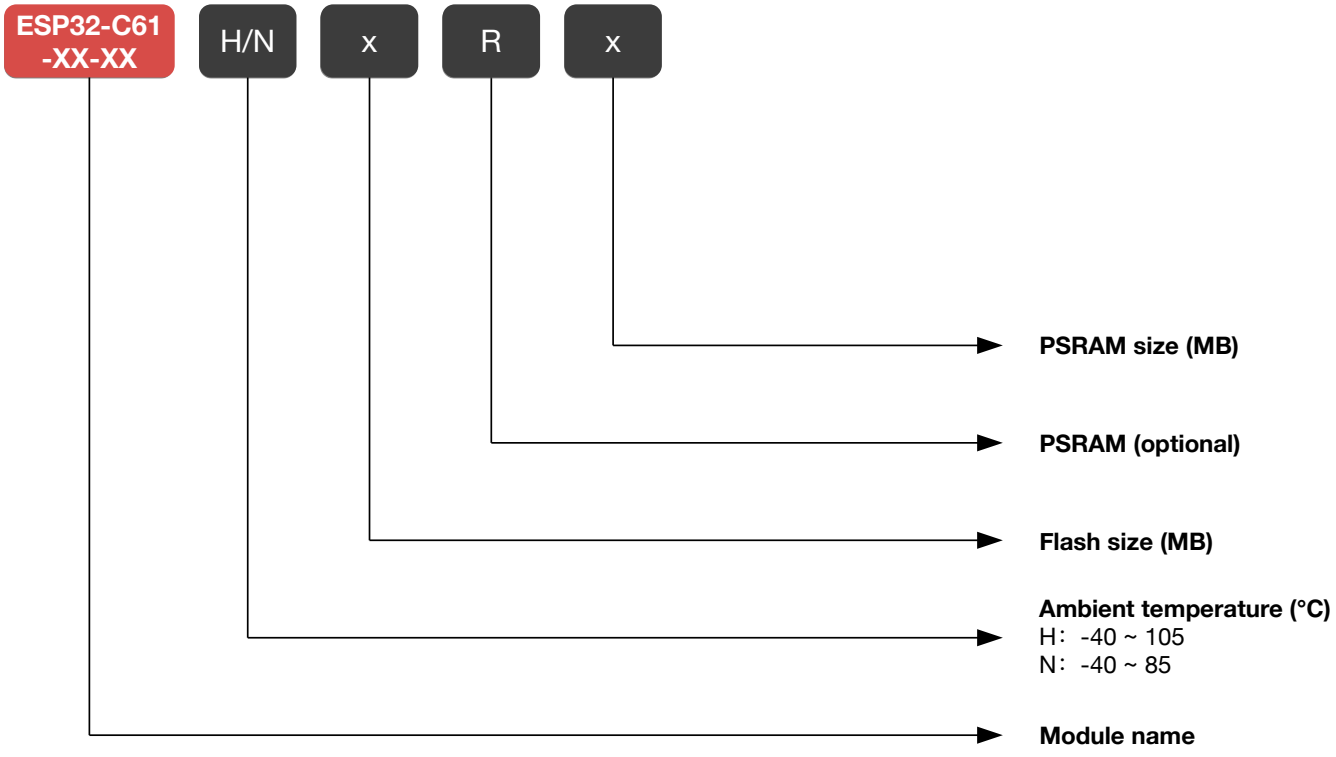

Figure 1: ESP32-C61 Module Variant Nomenclature

The series comparison for the two modules is as follows:

Table 1: ESP32-C61-WROOM-1 (ANT) Series Comparison[1]

Part Number[2]	Flash [3]	PSRAM	Embedded Chip	Ambient Temp.[4] (°C)	Size[5] (mm)
ESP32-C61-WROOM-1-N8R2	8 MB (Quad SPI)	2 MB	ESP32-C61HR2	−40 ~ 85	18.0 × 25.5 × 3.1
ESP32-C61-WROOM-1-N8R8	8 MB (Quad SPI)	8 MB	ESP32-C61HR8	−40 ~ 85	18.0 × 25.5 × 3.1

[1] This table shares the same notes presented in Table 2 below.

Table 2: ESP32-C61-WROOM-1U (CONN) Series Comparison

Part Number[2]	Flash [3]	PSRAM	Embedded Chip	Ambient Temp.[4] (°C)	Size[5] (mm)
ESP32-C61-WROOM-1U-N8R2	8 MB (Quad SPI)	2 MB	ESP32-C61HR2	−40 ~ 85	18.0 × 19.2 × 3.2
ESP32-C61-WROOM-1U-N8R8	8 MB (Quad SPI)	8 MB	ESP32-C61HR8	−40 ~ 85	
ESP32-C61-WROOM-1U-H16R2	16 MB (Quad SPI)	2 MB	ESP32-C61HR2	−40 ~ 105	

[2] Variants with special flash, PSRAM sizes, or ambient temperatures are not listed individually. The flash can be customized up to 16 MB and the PSRAM can be customized up to 8 MB. For customization requests, please contact us. For module variants not listed, refer to Figure 1 *ESP32-C61 Module Variant Nomenclature* for the specific specifications.

[3] For specifications, refer to Section 6.5 *Memory Specifications*.

[4] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[5] For details, refer to Section 10.1 *Module Dimensions*.

[6] ESP32-C61-WROOM-1U uses ANT1 by default. To order the ANT2 model, add T2 to the general Part Number, for example: ESP32-C61-WROOM-1U-N8R2T2.

At the core of the modules is ESP32-C61 *, a 32-bit RISC-V single-core processor.

Note:
For more information on ESP32-C61, please refer to *ESP32-C61 Series Datasheet*.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

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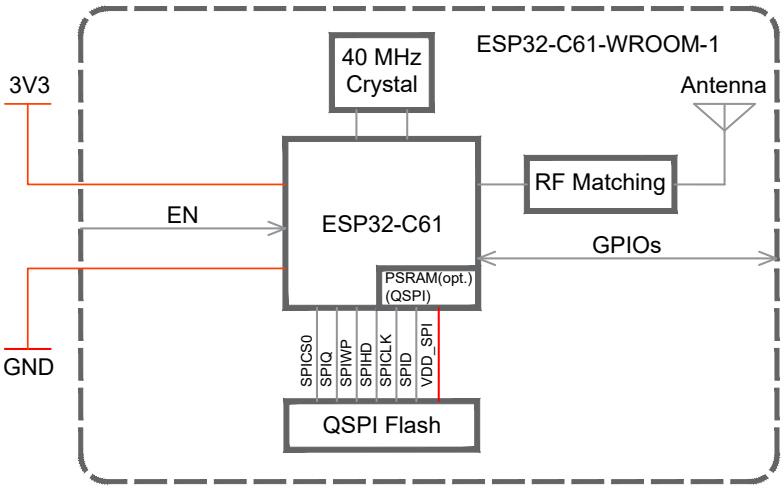

Figure 2: ESP32-C61-WROOM-1 Block Diagram

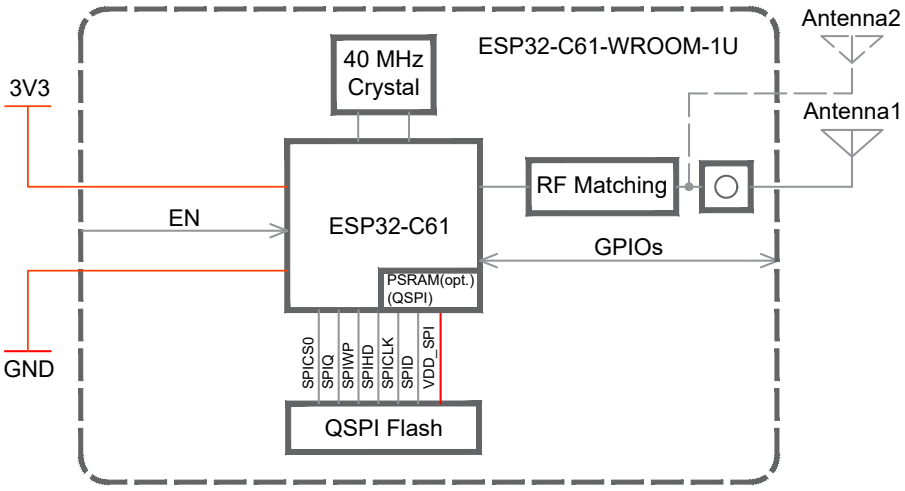

Figure 3: ESP32-C61-WROOM-1U Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10.1 *Module Dimensions*.

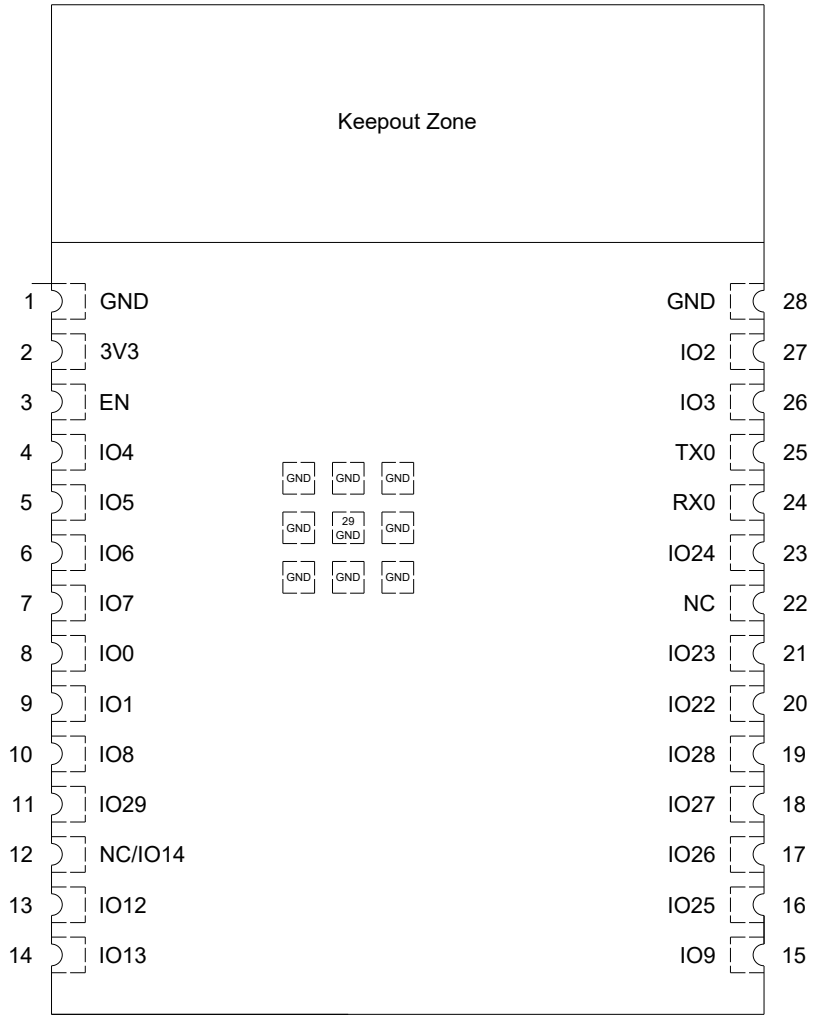

Figure 4: ESP32-C61-WROOM-1 Pin Layout (Top View)

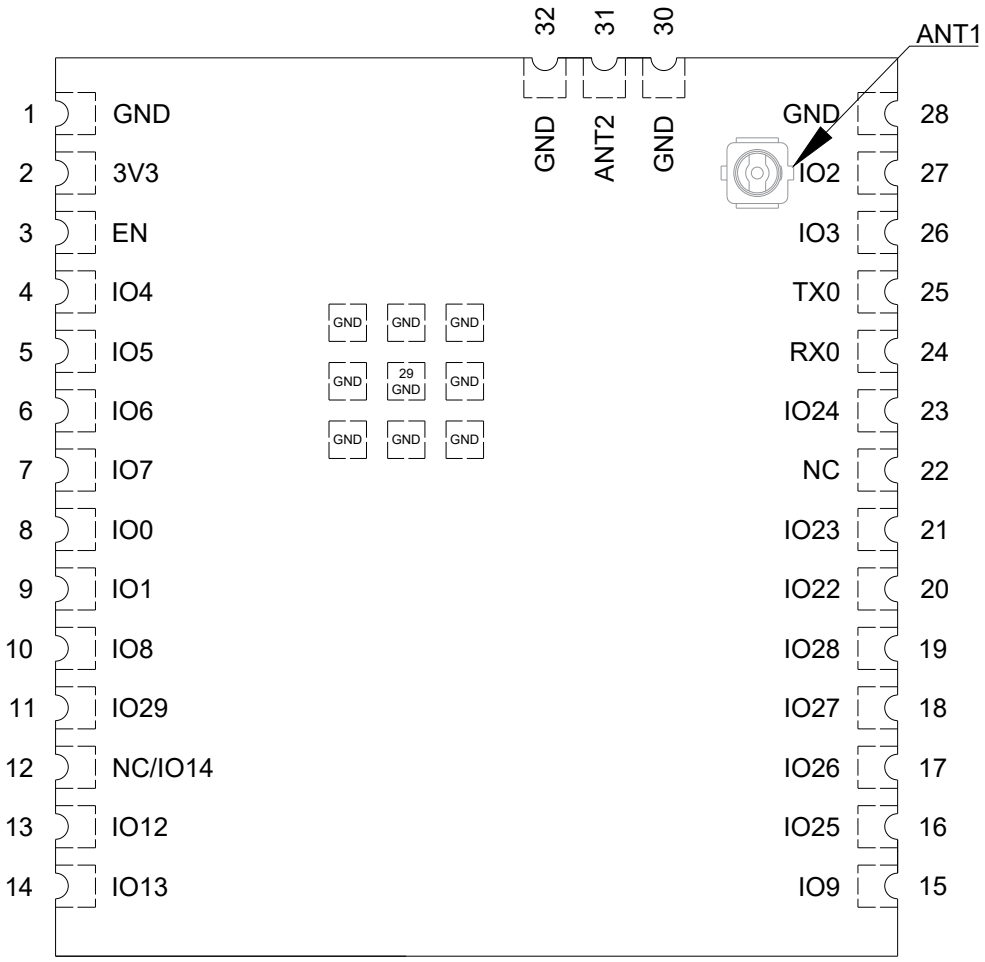

Figure 5: ESP32-C61-WROOM-1U Pin Layout (Top View)

3.2 Pin Description

ESP32-C61-WROOM-1 module has 29 pins and ESP32-C61-WROOM-1U module has 32 pins. See pin definitions in Table 3 *Pin Description* and Table 4 *Pin Description*.

For peripheral pin configurations, please refer to *ESP32-C61 Series Datasheet*.

Table 3: ESP32-C61-WROOM-1 Pin Definitions[1]

Name	No.	Type[2]	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	MTDI, GPIO4, LP_GPIO4, ADC1_CH2, FSPIWP
IO5	5	I/O/T	MTCK, GPIO5, LP_GPIO5, ADC1_CH3
IO6	6	I/O/T	MTDO, GPIO6, LP_GPIO6, FSPICLK
IO7	7	I/O/T	GPIO7, FSPID
IO0	8	I/O/T	XTAL_32K_P, GPIO0, LP_GPIO0

Cont'd on next page

Table 3 – cont'd from previous page

Name	No.	Type[2]	Function
IO1	9	I/O/T	XTAL_32K_N, GPIO1, LP_GPIO1, ADC1_CH0
IO8	10	I/O/T	GPIO8, ZCD0, FSPICS0
IO29	11	I/O/T	GPIO29
NC/IO14	12	I/O/T	NC/**GPIO14**[3]
IO12	13	I/O/T	USB_D-, GPIO12
IO13	14	I/O/T	USB_D+, GPIO13
IO9	15	I/O/T	GPIO9, ZCD1
IO25	16	I/O/T	GPIO25, SDIO_CMD
IO26	17	I/O/T	GPIO26, SDIO_CLK
IO27	18	I/O/T	GPIO27, SDIO_DATA0
IO28	19	I/O/T	GPIO28, SDIO_DATA1
IO22	20	I/O/T	GPIO22, SDIO_DATA2
IO23	21	I/O/T	GPIO23, SDIO_DATA3
NC	22	—	NC
IO24	23	I/O/T	GPIO24
RX0	24	I/O/T	U0RXD, GPIO10
TX0	25	I/O/T	U0TXD, GPIO11
IO3	26	I/O/T	MTMS, GPIO3, LP_GPIO3, ADC1_CH1, FSPIHD
IO2	27	I/O/T	GPIO2, LP_GPIO2, FSPIQ
GND	28	P	Ground
EPAD	29	P	Ground

[1] This table shares the notes 2 and 3 presented in Table 4 below.

Table 4: ESP32-C61-WROOM-1U Pin Definitions

Name	No.	Type[2]	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	MTDI, GPIO4, LP_GPIO4, ADC1_CH2, FSPIWP
IO5	5	I/O/T	MTCK, GPIO5, LP_GPIO5, ADC1_CH3
IO6	6	I/O/T	MTDO, GPIO6, LP_GPIO6, FSPICLK
IO7	7	I/O/T	GPIO7, FSPID
IO0	8	I/O/T	XTAL_32K_P, GPIO0, LP_GPIO0
IO1	9	I/O/T	XTAL_32K_N, GPIO1, LP_GPIO1, ADC1_CH0
IO8	10	I/O/T	GPIO8, ZCD0, FSPICS0
IO29	11	I/O/T	GPIO29
NC/IO14	12	I/O/T	NC/**GPIO14**[3]
IO12	13	I/O/T	USB_D-, GPIO12

Cont'd on next page

Table 4 – cont'd from previous page

Name	No.	Type[2]	Function
IO13	14	I/O/T	USB_D+, GPIO13
IO9	15	I/O/T	GPIO9, ZCD1
IO25	16	I/O/T	GPIO25, SDIO_CMD
IO26	17	I/O/T	GPIO26, SDIO_CLK
IO27	18	I/O/T	GPIO27, SDIO_DATA0
IO28	19	I/O/T	GPIO28, SDIO_DATA1
IO22	20	I/O/T	GPIO22, SDIO_DATA2
IO23	21	I/O/T	GPIO23, SDIO_DATA3
NC	22	—	NC
IO24	23	I/O/T	GPIO24
RX0	24	I/O/T	U0RXD, GPIO10
TX0	25	I/O/T	U0TXD, GPIO11
IO3	26	I/O/T	MTMS, GPIO3, LP_GPIO3, ADC1_CH1, FSPIHD
IO2	27	I/O/T	GPIO2, LP_GPIO2, FSPIQ
GND	28	P	Ground
EPAD	29	P	Ground
GND	30	P	Ground
ANT2[4]	31	I/O	RF input and output
GND	32	P	Ground

[2] P: power supply; I: input; O: output; T: high impedance.

[3] In modules with embedded SPI PSRAM, this pin is already used as SPICS1 for SPI PSRAM and cannot be used for other functions. In modules without embedded SPI PSRAM, this pin can be used as GPIO14.

[4] By default, ESP32-C61-WROOM-1U uses ANT1, and ANT2 is disabled. To use ANT2, please contact us.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-C61 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping-pins and eFuse parameter at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO8 and GPIO9
- **SDIO sampling and driving clock edge**
  - Strapping pin: MTDI and MTMS
- **ROM message printing**
  - Strapping pin: GPIO8
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
- **JTAG signal source**
  - Strapping pin: GPIO7
  - eFuse parameter: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 5: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
MTMS	Floating	–
MTDI	Floating	–
GPIO7	Floating	–
GPIO8	Floating	–
GPIO9	Pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-C61 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in

any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 6 and Figure 6.

Table 6: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

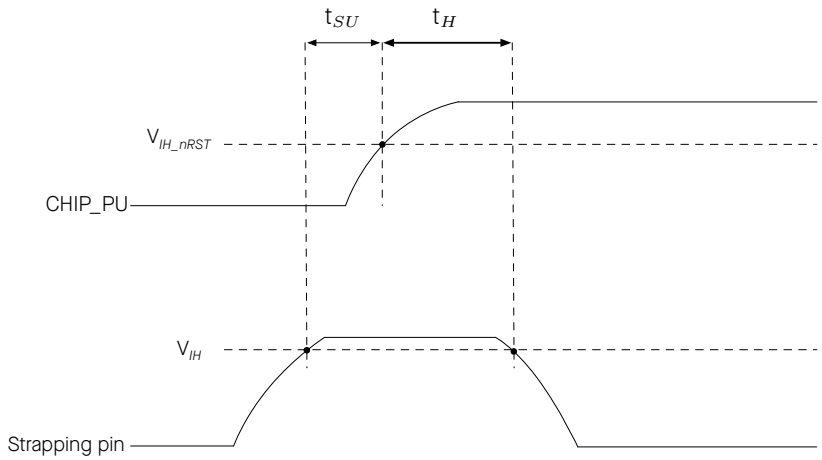

Figure 6: Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 7 *Chip Boot Mode Control*.

Table 7: Chip Boot Mode Control

Boot Mode	GPIO8	GPIO9
SPI Boot [1]	Any value	1
Joint Download Boot[2]	1	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SDIO Slave 2.0 Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0, USB or SDIO Slave interfaces and execute it in SPI Boot mode.

In Joint Download Boot mode, it is also possible to download binary files into SRAM using UART0, USB or SDIO Slave interfaces and execute it from SRAM.

4.2 SDIO Sampling and Driving Clock Edge Control

The strapping pin MTMS and MTDI can be used to decide on which clock edge to sample signals and drive output lines. See Table 8 SDIO Input Sampling Edge/Output Driving Edge Control.

Table 8: SDIO Input Sampling Edge/Output Driving Edge Control

Edge behavior	MTMS	MTDI
Falling edge sampling, falling edge output	0	0
Falling edge sampling, rising edge output	0	1
Rising edge sampling, falling edge output	1	0
Rising edge sampling, rising edge output	1	1

[1] MTMS and MTDI are floating by default, so above are not default configurations.

4.3 ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

LP_AON_STORE4_REG[0], EFUSE_UART_PRINT_CONTROL and GPIO8 control ROM messages printing to **UART0** as shown in Table 9 *UART0 ROM Message Printing Control*.

Table 9: UART0 ROM Message Printing Control

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8	Register[1]
Always enabled[2]	**0**	Ignored	0
Enabled	1	0	
Disabled		1	
Disabled	2	0	
Enabled		1	
Always disabled	3	Ignored	
Disabled	Ignored	Ignored	1

[1] Register: LP_AON_STORE4_REG[0]

[2] **Bold** marks the default value and configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT and LP_AON_STORE4_REG[0] control the printing to **USB Serial/JTAG controller** as shown in Table 10 *USB Serial/JTAG ROM Message Printing Control*.

Table 10: USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Message Printing Control	LP_AON_STORE4_REG[0]	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled	**0**	**0**
Disabled	0	1
	1	Ignored

[1] **Bold** marks the default value and configuration.

4.4 JTAG Signal Source Control

The strapping pin GPIO7 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 11 shows, GPIO7 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

Table 11: JTAG Signal Source Control

eFuse 1[1]	eFuse 2[2]	eFuse 3[3]	GPIO7	JTAG Signal Source
0	**0**	**0**	x[4]	**USB Serial/JTAG Controller**[5]
		1	1	
			0	JTAG pins MTDI, MTCK, MTMS and MTDO
0	x	x	x	
0	1	x	x	
1	0	x	x	USB Serial/JTAG Controller
1	1	x	x	JTAG is disabled
1	x	x	x	

[1] **eFuse 1**: EFUSE_DIS_PAD_JTAG

[2] **eFuse 2**: EFUSE_DIS_USB_JTAG

[3] **eFuse 3**: EFUSE_JTAG_SEL_ENABLE

[4] x: x indicates that the value has no effect on the result and can be ignored.

[5] **Bold** marks the default value and configuration.

5 Peripherals

5.1 Functional Overview

ESP32-C61 integrates a rich set of peripherals including GPIO, SPI, UART, I2C, I2S, LED PWM, USB Serial/JTAG controller, GDMA, On-chip debug functionality via JTAG, event task matrix, ADC, temperature sensor, brown-out detector, analog voltage comparator, general-purpose timers, system timer, and watchdog timers etc.

To learn more about on-chip components, please refer to *ESP32-C61 Series Datasheet* > Section *Functional Description*.

Note:
The content below is sourced from *ESP32-C61 Series Datasheet* > Section *Peripherals*. Some information may not be applicable to ESP32-C61-WROOM-1 and ESP32-C61-WROOM-1U as not all the IO signals are exposed on the module. To learn more about peripheral signals, please refer to *ESP32-C61 Technical Reference Manual* > Section *Peripheral Signal List*.

5.2 Peripheral Description

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

5.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

5.2.1.1 UART Controller

The UART Controller in the ESP32-C61 chip facilitates the transmission and reception of asynchronous serial data between the chip and external UART devices. It supports three UART interfaces.

Feature List

- Programmable baud rates up to 5 MBaud
- RAM shared by TX FIFOs and RX FIFOs
- Support for various lengths of data bits and stop bits
- Parity bit support
- Special character AT_CMD detection
- RS485 protocol support
- IrDA protocol support
- High-speed data communication using GDMA
- Receive timeout feature

- UART as the wake-up source
- Software and hardware flow control

Pin Assignment

The pins connected to transmit and receive signals (U0TXD and U0RXD) for **UART0** are multiplexed with GPIO10 ~ GPIO11 via IO MUX. Other signals can be routed to any GPIOs via the GPIO matrix.

5.2.1.2 SPI Controller

ESP32-C61 has the following SPI interfaces:

- **SPI0** used by ESP32-C61's cache and GDMA to access in-package or off-package flash/PSRAM
- **SPI1** used by the CPU to access in-package or off-package flash/PSRAM
- **SPI2** is a general-purpose SPI controller with access to general-purpose DMA channels

SPI0 and SPI1 are reserved for system use, and only SPI2 is available for users.

Features of SPI0 and SPI1

- Supports Single SPI, Dual SPI, Quad SPI, QPI modes
- Data transmission is in bytes

Features of SPI2

- Supports operation as a master or slave
- Support for DMA
- Supports Single SPI, Dual SPI, Quad SPI, QPI modes
- Configurable clock polarity (CPOL) and phase (CPHA)
- Configurable clock frequency
- Data transmission is in bytes
- Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first
- As a master
  - Supports 2-line full-duplex communication with clock frequency up to 80 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 80 MHz
  - Provides six FSPICS... pins for connection with six independent SPI slaves
  - Configurable CS setup time and hold time
- As a slave
  - Supports 2-line full-duplex communication with clock frequency up to 60 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 60 MHz

Pin Assignment

For SPI0/1, the pins are multiplexed with GPIO14 ~ GPIO17 and GPIO19 ~ GPIO20 via the IO MUX.

For SPI2, the pins for data and clock signals are multiplexed with GPIO2, GPIO7, and JTAG interface via the IO MUX. The pins for chip select signals for multiplexed with GPIO8 via the IO MUX.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.1.3 I2C Controller

The I2C Controller supports communication between the master and slave devices using the I2C bus.

Feature List

- Communication with multiple external devices
- Master and slave modes for I2C
- Standard mode (100 Kbit/s) and fast mode (400 Kbit/s)
- SCL clock stretching in slave mode
- Programmable digital noise filtering
- Support for 7-bit and 10-bit addressing, as well as dual address mode

Pin Assignment

For regular I2C, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.1.4 I2S Controller

The I2S Controller in the ESP32-C61 chip provides a flexible communication interface for streaming digital data in multimedia applications, particularly digital audio applications.

Feature List

- Master mode and slave mode
- Full-duplex and half-duplex communications
- Separate TX and RX units that can work independently or simultaneously
- A variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- PCM-to-PDM TX interface
- Configurable high-precision BCK clock, with frequency up to 40 MHz

  - Sampling frequencies can be 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 128 kHz, 192 kHz, etc.
- 8-/16-/24-/32-bit data communication
- Direct Memory Access (DMA)
- A-law and μ-law compression/decompression algorithms for improved signal-to-quantization noise ratio
- Flexible data format control

Pin Assignment

The pins for the I2S Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.1.5 USB Serial/JTAG Controller

The USB Serial/JTAG controller in the ESP32-C61 chip provides an integrated solution for communicating to the chip over a standard USB CDC-ACM serial port as well as a convenient method for JTAG debugging. It eliminates the need for external chips or JTAG adapters, saving space and reducing cost.

Feature List

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)
- CDC-ACM virtual serial port and JTAG adapter functionality
- CDC-ACM:
  - CDC-ACM adherent serial port emulation (plug-and-play on most modern OSes)
  - Host controllable chip reset and entry into download mode
- JTAG adapter functionality:
  - Fast communication with CPU debugging core using a compact representation of JTAG instructions
- Support for reprogramming of attached flash memory through the ROM startup code
- Internal PHY

Pin Assignment

The pins for the USB Serial/JTAG Controller are multiplexed with GPIO12 ~ GPIO13 via IO MUX.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.1.6 LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels. The LED PWM controller supports:

Feature List

- Generating digital waveform with configurable periods and duty cycle. The resolution of duty cycle can be up to 20 bits
- Multiple clock sources, including 80 MHz PLL clock, external main crystal clock, and internal fast RC oscillator
- Operation when the CPU is in Light-sleep mode
- Gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator
- Up to 16 duty cycle ranges for gamma curve generation, each can be independently configured in terms of duty cycle direction (increase or decrease), step size, the number of steps, and step frequency

Pin Assignment

The pins for the LED PWM Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.1.7 SDIO Slave Controller

The SDIO Slave controller in ESP32-C61 provides hardware support for the Secure Digital Input/Output (SDIO) device interface. It allows an SDIO host to access ESP32-C61 via an SDIO bus protocol.

Feature List

- compatible with SDIO Physical Layer Specification V2.00 and SDIO Specifications V2.00
- support SPI, 1-bit SDIO, and 4-bit SDIO transfer modes
- clock range of 0 ~ 50 MHz
- configurable sample and drive clock edge
- integrated and SDIO-accessible registers for information interaction
- support SDIO interrupts
- automatic padding data and discarding the padded data on the SDIO bus
- block size up to 512 bytes
- interrupt vector between the host and slave for bidirectional interrupt
- support DMA for data transfer
- support wake-up from sleep when connection is retained

Pin Assignment

The pins for the SDIO Slave controller are multiplexed with GPIO22 ~ GPIO23, and GPIO25 ~ GPIO28 via IO MUX.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

5.2.2.1 SAR ADC

ESP32-C61 integrates a Successive Approximation Analog-to-Digital Converter (SAR ADC) to convert analog signals into digital representations.

Feature List

- 12-bit sampling resolution
- Analog voltage sampling from up to four pins
- Attenuation of input signals for voltage conversion
- Software-triggered one-time sampling
- Timer-triggered multi-channel scanning
- DMA continuous conversion for seamless data transfer
- Two filters with configurable filter coefficient
- Threshold monitoring which helps to trigger an interrupt
- Support for Event Task Matrix

Pin Assignment

The SAR ADC pins are multiplexed with GPIO1 and GPIO3 ~ GPIO5. These GPIOs are also multiplexed with LP_GPIO1, LP_GPIO3 ~ LP_GPIO5, and with the JTAG interface.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

5.2.2.2 Temperature Sensor

The Temperature Sensor in the ESP32-C61 chip allows for real-time monitoring of temperature changes inside the chip.

Feature List

- Measurement range: −40°C ~ 125°C
- Software triggering, wherein the data can be read continuously once triggered
- Hardware automatic triggering and temperature monitoring
- Configurable temperature offset based on the environment to improve the accuracy
- Adjustable measurement range
- Two automatic monitoring wake-up modes: absolute value mode and incremental value mode
- Support for Event Task Matrix

5.2.2.3 Analog Voltage Comparator

ESP32-C61 provides a group of analog voltage comparators which contain two special pads. This peripheral can be used to compare the voltages of the two pads or compare the voltage of one pad with an internally adjustable stable voltage.

Feature List

- Internal or external reference voltage
- Supported internal reference voltage ranging from 0 to 0.7 × VDD_PST
- Support for ETM
- Interrupt triggered when the measured voltage reaches the reference voltage

Pin Assignment

The analog voltage comparator has dedicated pads, GPIO8 and GPIO9. GPIO9 is the test pad, and GPIO8 serves as the reference pad when using an external reference voltage.

For more information about the pin assignment, see *ESP32-C61 Series Datasheet* > Section *IO Pins*.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 12 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 13 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 12: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V

6.2 Recommended Operating Conditions

Table 13: Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
VDD33	Power supply voltage		3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply		0.5	—	—	A
T_A	Operating ambient temperature	85 °C version	−40	—	85	°C
		105 °C version			105	

6.3 DC Characteristics (3.3 V, 25 °C)

Table 14: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage	−0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.
[2] V_{OH} and V_{OL} are measured using high-impedance load.

6.4 Current Consumption Characteristics

6.4.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 15: Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, DSSS @20.5 dBm	370
		802.11g, 54 Mbps, OFDM @18.5 dBm	307
		802.11n, HT20, MCS7 @17.5 dBm	285
		802.11n, HT40, MCS7 @17 dBm	267
		802.11ax, MCS9 @14.5 dBm	238
	RX	802.11b/g/n, HT20	88
		802.11n, HT40	90
		802.11ax, HE20	88

Table 16: Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 18 dBm	300
		Bluetooth LE @ 9 dBm	166
		Bluetooth LE @ 0 dBm	135
		Bluetooth LE @ −15 dBm	96
	RX	Bluetooth LE	81

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-C61 Series Datasheet*.

6.4.2 Current Consumption in Other Modes

Table 17: Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ (mA)	
			All Peripherals Clocks Disabled	All Peripherals Clocks Enabled[1]
Modem-sleep[2,3]	160	WAITI	11	18

Table 17: Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ (mA)	
			All Peripherals Clocks Disabled	All Peripherals Clocks Enabled[1]
		CPU while loop	16	23
		Run CoreMark	21	28
	80	WAITI	10	16
		CPU while loop	12	19
		Run CoreMark	15	21
	40	WAITI	6	11
		CPU while loop	7	12
		Run CoreMark	9	13

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash.

Table 18: Current Consumption in Low-Power Modes

Mode	Description	Typ (mA)
Light-sleep	CPU and wireless communication modules are powered down, peripheral clocks are disabled, and all GPIOs are high-impedance	0.2
	CPU, wireless communication modules and peripherals are powered down, and all GPIOs are high-impedance	0.05
Deep-sleep	LP timer and LP memory are powered on	0.01
Power off	CHIP_PU is set to low level, the chip is powered off	0.001

6.5 Memory Specifications

The data below is sourced from the memory vendor datasheet. These values are guaranteed through design and/or characterization but are not fully tested in production. Devices are shipped with the memory erased.

Table 19: Flash Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.65	1.80	2.00	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz
—	Program/erase cycles	100,000	—	—	cycles
T_{RET}	Data retention time	20	—	—	years
T_{PP}	Page program time	—	0.8	5	ms
T_{SE}	Sector erase time (4 KB)	—	70	500	ms
T_{BE1}	Block erase time (32 KB)	—	0.2	2	s

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Table 19 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
T_{BE2}	Block erase time (64 KB)	—	0.3	3	s
T_{CE}	Chip erase time (16 Mb)	—	7	20	s
	Chip erase time (32 Mb)	—	20	60	s
	Chip erase time (64 Mb)	—	25	100	s
	Chip erase time (128 Mb)	—	60	200	s
	Chip erase time (256 Mb)	—	70	300	s

Table 20: PSRAM Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.62	1.80	1.98	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz

7 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance of 50 Ω.Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

7.1 Wi-Fi Radio (2.4 GHz)

Table 21: Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n/ax

7.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 22: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	20.5	—
802.11b, 11 Mbps, CCK	—	20.5	—
802.11g, 6 Mbps, OFDM	—	19.5	—
802.11g, 54 Mbps, OFDM	—	18.5	—
802.11n, HT20, MCS0	—	18.5	—
802.11n, HT20, MCS7	—	17.5	—
802.11n, HT40, MCS0	—	18.0	—
802.11n, HT40, MCS7	—	17.0	—
802.11ax, HE20, MCS0	—	18.5	—
802.11ax, HE20, MCS9	—	14.5	—

Table 23: TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	–24.8	–10.0
802.11b, 11 Mbps, CCK	—	–24.8	–10.0
802.11g, 6 Mbps, OFDM	—	–24.5	–5.0

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Table 23 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11g, 54 Mbps, OFDM	—	–29.0	–25.0
802.11n, HT20, MCS0	—	–23.0	–5.0
802.11n, HT20, MCS7	—	–31.4	–27.0
802.11n, HT40, MCS0	—	–25.8	–5.0
802.11n, HT40, MCS7	—	–30.5	–27.0
802.11ax, HE20, MCS0	—	–23.0	–5.0
802.11ax, HE20, MCS9	—	–34.0	–32.0

[1] EVM is measured at the corresponding typical TX power provided in Table *22 Wi-Fi RF Transmitter (TX) Characteristics* above.

7.1.2 Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n/ax.

Table 24: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–99.5	—
802.11b, 2 Mbps, DSSS	—	–96.0	—
802.11b, 5.5 Mbps, CCK	—	–93.5	—
802.11b, 11 Mbps, CCK	—	–90.0	—
802.11g, 6 Mbps, OFDM	—	–94.0	—
802.11g, 9 Mbps, OFDM	—	–93.0	—
802.11g, 12 Mbps, OFDM	—	–92.0	—
802.11g, 18 Mbps, OFDM	—	–89.5	—
802.11g, 24 Mbps, OFDM	—	–86.5	—
802.11g, 36 Mbps, OFDM	—	–83.0	—
802.11g, 48 Mbps, OFDM	—	–78.5	—
802.11g, 54 Mbps, OFDM	—	–77.5	—
802.11n, HT20, MCS0	—	–94.0	—
802.11n, HT20, MCS1	—	–92.0	—
802.11n, HT20, MCS2	—	–89.5	—
802.11n, HT20, MCS3	—	–86.0	—
802.11n, HT20, MCS4	—	–83.0	—
802.11n, HT20, MCS5	—	–78.5	—
802.11n, HT20, MCS6	—	–77.0	—
802.11n, HT20, MCS7	—	–75.0	—
802.11n, HT40, MCS0	—	–91.0	—
802.11n, HT40, MCS1	—	–89.5	—
802.11n, HT40, MCS2	—	–87.0	—

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Table 24 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS3	—	–83.5	—
802.11n, HT40, MCS4	—	–80.5	—
802.11n, HT40, MCS5	—	–76.0	—
802.11n, HT40, MCS6	—	–74.0	—
802.11n, HT40, MCS7	—	–73.0	—
802.11ax, HE20, MCS0	—	–93.5	—
802.11ax, HE20, MCS1	—	–91.0	—
802.11ax, HE20, MCS2	—	–88.0	—
802.11ax, HE20, MCS3	—	–85.0	—
802.11ax, HE20, MCS4	—	–82.0	—
802.11ax, HE20, MCS5	—	–78.0	—
802.11ax, HE20, MCS6	—	–76.0	—
802.11ax, HE20, MCS7	—	–74.5	—
802.11ax, HE20, MCS8	—	–71.0	—
802.11ax, HE20, MCS9	—	–68.0	—

Table 25: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	5	—
802.11g, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—
802.11ax, HE20, MCS0	—	5	—
802.11ax, HE20, MCS9	—	0	—

Table 26: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	38	—
802.11b, 11 Mbps, CCK	—	38	—
802.11g, 6 Mbps, OFDM	—	33	—
802.11g, 54 Mbps, OFDM	—	16	—
802.11n, HT20, MCS0	—	32	—

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Table 26 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11n, HT20, MCS7	—	17	—
802.11n, HT40, MCS0	—	24	—
802.11n, HT40, MCS7	—	13	—
802.11ax, HE20, MCS0	—	37	—
802.11ax, HE20, MCS9	—	13	—

7.2 Bluetooth 5 (LE) Radio

Table 27: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–15 ~ 20 dBm

7.2.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 28: Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	10.9	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	3.5	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	2.4	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	2.7	—	kHz
Modulation characteristics	$\Delta\, F1_{\text{avg}}$	—	250.0	—	kHz
	Min. $\Delta\, F2_{\text{max}}$ (for at least 99.9% of all $\Delta\, F2_{\text{max}}$)	—	243.0	—	kHz
	$\Delta\, F2_{\text{avg}} / \Delta\, F1_{\text{avg}}$	—	0.88	—	—
In-band emissions	± 2 MHz offset	—	–27	—	dBm
	± 3 MHz offset	—	–36	—	dBm
	> ± 3 MHz offset	—	–42	—	dBm

Table 29: Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	9.4	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	3.7	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.1	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	3.3	—	kHz
Modulation characteristics	$\Delta\, F1_{\text{avg}}$	—	499.4	—	kHz

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Table 29 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	–	532.0	–	kHz
	$\Delta F2_{avg}/\Delta F1_{avg}$	–	0.95	–	–
In-band emissions	± 4 MHz offset	–	–41	–	dBm
	± 5 MHz offset	–	–44	–	dBm
	> ± 5 MHz offset	–	–45	–	dBm

Table 30: Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	10.1	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	2.1	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	1.2	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	0.7	–	kHz
Modulation characteristics	$\Delta F1_{avg}$	–	253.1	–	kHz
	Min. $\Delta F1_{max}$ (for at least 99.9% of all $\Delta F1_{max}$)	–	270.5	–	kHz
In-band emissions	± 2 MHz offset	–	–27	–	dBm
	± 3 MHz offset	–	–38	–	dBm
	> ± 3 MHz offset	–	–43	–	dBm

Table 31: Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	10.2	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	1.2	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	0.6	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	1.8	–	kHz
Modulation characteristics	$\Delta F2_{avg}$	–	223.4	–	kHz
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	–	243.5	–	kHz
In-band emissions	± 2 MHz offset	–	–27	–	dBm
	± 3 MHz offset	–	–37	–	dBm
	> ± 3 MHz offset	–	43	–	dBm

7.2.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 32: Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	–	–	–98.0	–	dBm
Maximum received signal @30.8% PER	–	–	8	–	dBm

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Table 32 – cont'd from previous page

Parameter		Description	Min	Typ	Max	Unit
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	7	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–2	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–34	—	dB
		F = F0 – 2 MHz	—	–27	—	dB
		F = F0 + 3 MHz	—	–33	—	dB
		F = F0 – 3 MHz	—	–40	—	dB
		F ≥ F0 + 4 MHz	—	–27	—	dB
		F ≤ F0 – 4 MHz	—	–53	—	dB
	Image frequency	—	—	–35	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–34	—	dB
		F = F_{image} – 1 MHz	—	–33	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–20	—	dBm
		2003 MHz ~ 2399 MHz	—	–25	—	dBm
		2484 MHz ~ 2997 MHz	—	–25	—	dBm
		3000 MHz ~ 12.75 GHz	—	–10	—	dBm
Intermodulation		—	—	–32	—	dBm

Table 33: Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–94.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	9	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	–7	—	dB
		F = F0 – 2 MHz	—	–6	—	dB
		F = F0 + 4 MHz	—	–21	—	dB
		F = F0 – 4 MHz	—	–27	—	dB
		F = F0 + 6 MHz	—	–38	—	dB
		F = F0 – 6 MHz	—	–41	—	dB
		F ≥ F0 + 8 MHz	—	–46	—	dB
		F ≤ F0 – 8 MHz	—	–46	—	dB
	Image frequency	—	—	–21	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–38	—	dB
		F = F_{image} – 2 MHz	—	–7	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–25	—	dBm
		2003 MHz ~ 2399 MHz	—	–25	—	dBm
		2484 MHz ~ 2997 MHz	—	–25	—	dBm
		3000 MHz ~ 12.75 GHz	—	–10	—	dBm
Intermodulation		—	—	–31	—	dBm

Table 34: Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–105.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–2	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–33	—	dB
		F = F0 – 2 MHz	—	–36	—	dB
		F = F0 + 3 MHz	—	–35	—	dB
		F = F0 – 3 MHz	—	–50	—	dB
		F $\geq$ F0 + 4 MHz	—	–31	—	dB
		F $\leq$ F0 – 4 MHz	—	–50	—	dB
	Image frequency	—	—	–31	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–35	—	dB

Table 35: Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–102.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–4	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–32	—	dB
		F = F0 – 2 MHz	—	–36	—	dB
		F = F0 + 3 MHz	—	–35	—	dB
		F = F0 – 3 MHz	—	–50	—	dB
		F $\geq$ F0 + 4 MHz	—	–29	—	dB
		F $\leq$ F0 – 4 MHz	—	–50	—	dB
	Image frequency	—	—	–29	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–35	—	dB

8 Module Schematics

This is the reference design of the module.

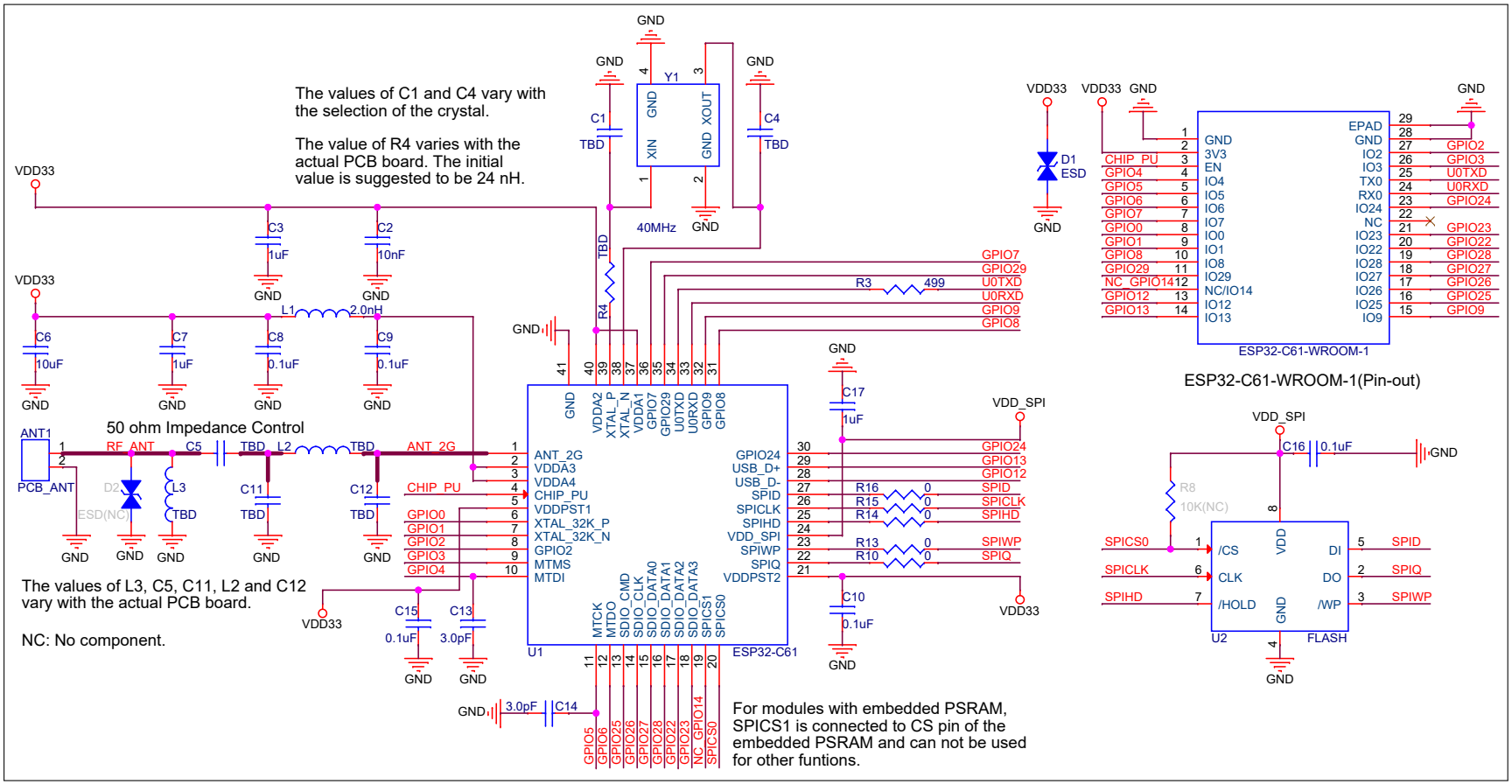

Figure 7: ESP32-C61-WROOM-1 Schematics

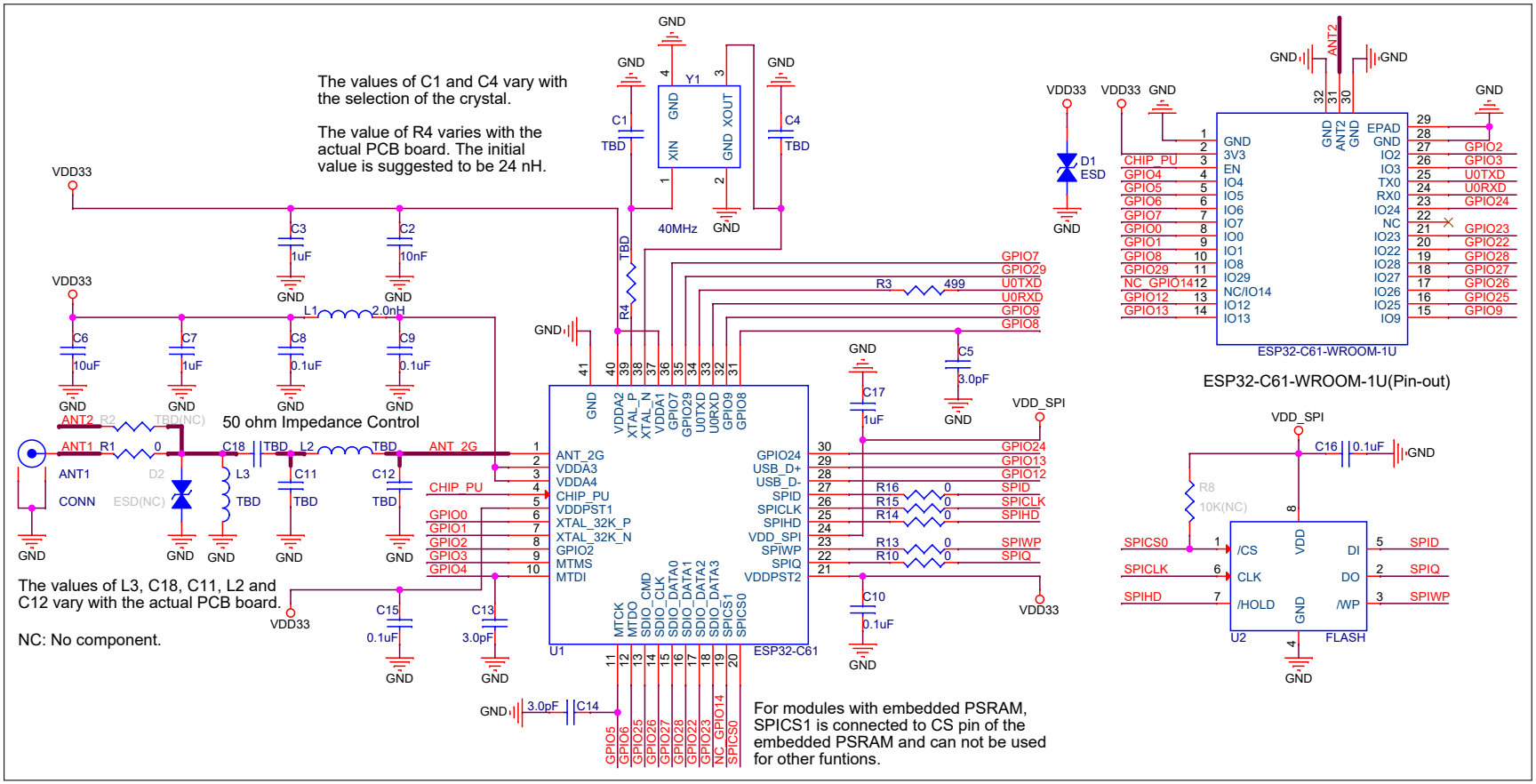

Figure 8: ESP32-C61-WROOM-1U Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, and UART interface).

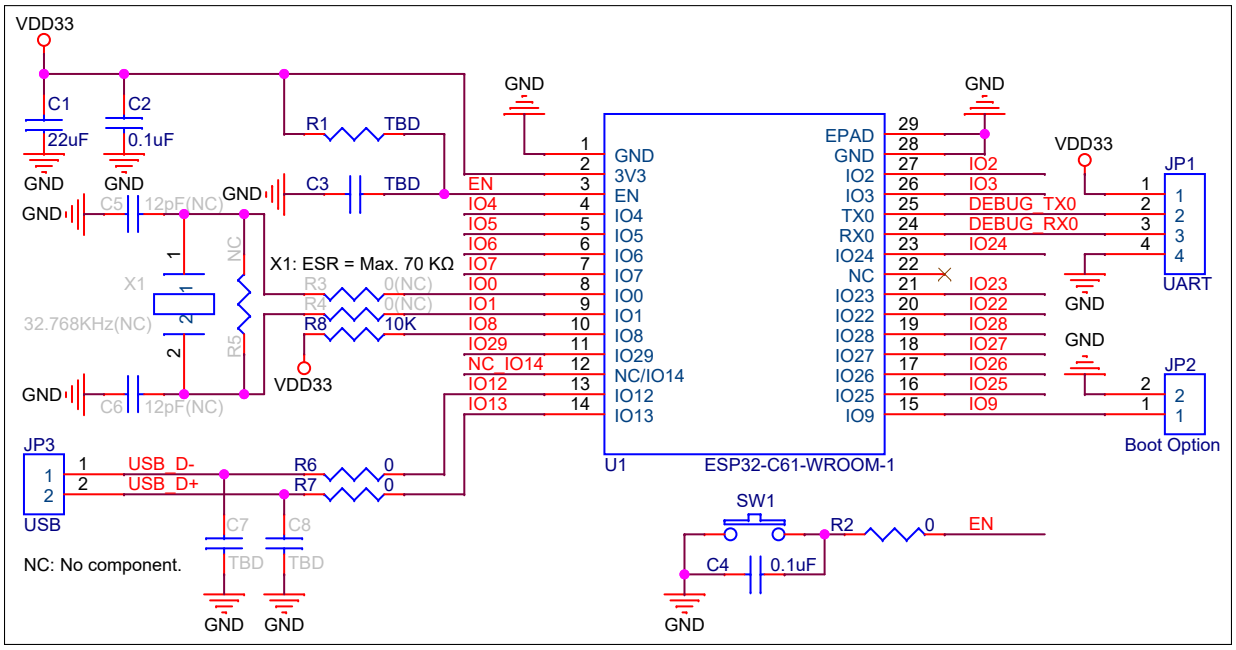

Figure 9: ESP32-C61-WROOM-1 Peripheral Schematics

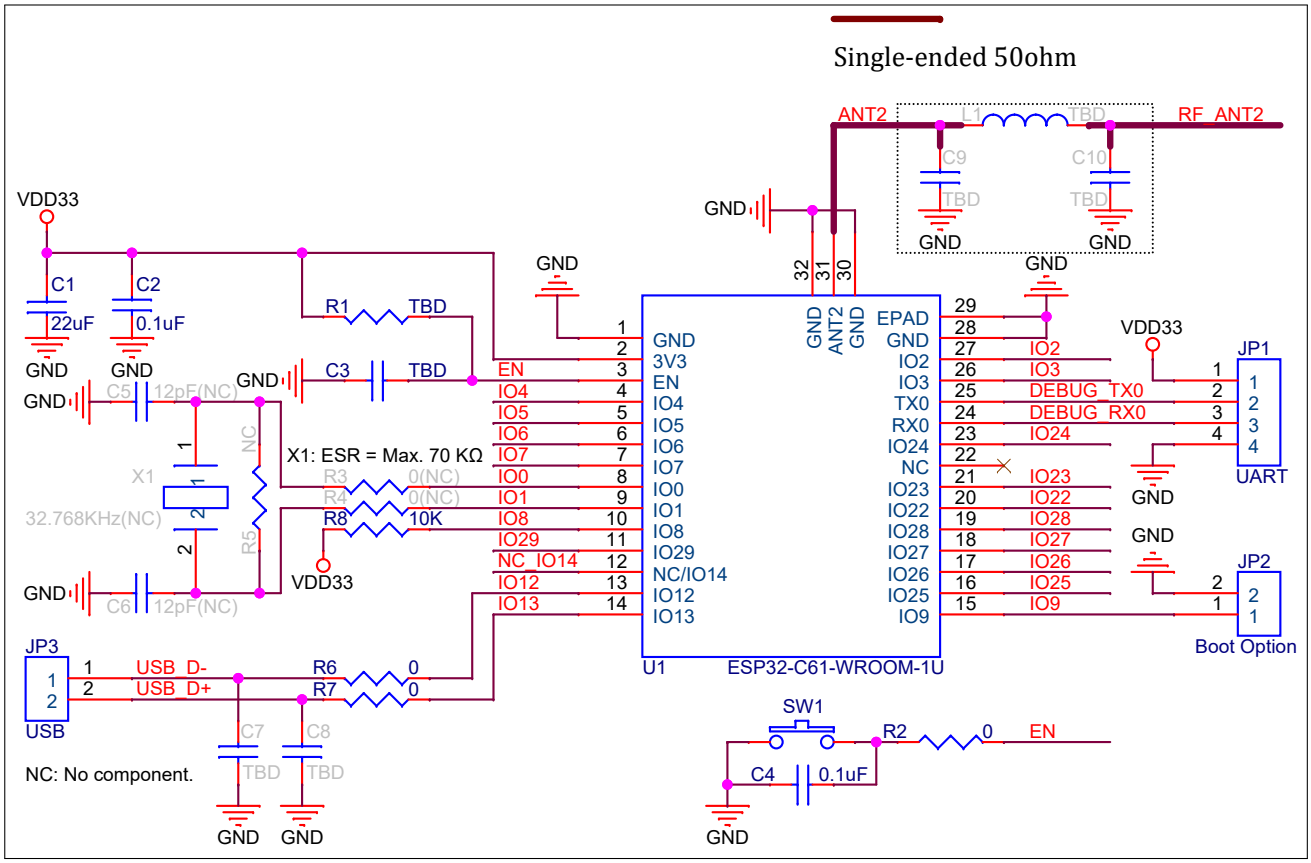

Figure 10: ESP32-C61-WROOM-1U Peripheral Schematics

- If an external antenna ANT2 is used, it is recommended to reserve an RF circuit as shown in the figure above. By default, ESP32-C61-WROOM-1U uses ANT1, and ANT2 is disabled. To use ANT2, please contact us.
- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-C61 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-C61's power-up and reset sequence timing diagram, please refer to *ESP32-C61 Series Datasheet* > Section *Power Supply*.
- UART0 is used to download firmware and log output. When using the AT firmware, please note that the UART GPIO is already configured . It is recommended to use the default configuration.

10 Physical Dimensions

10.1 Module Dimensions

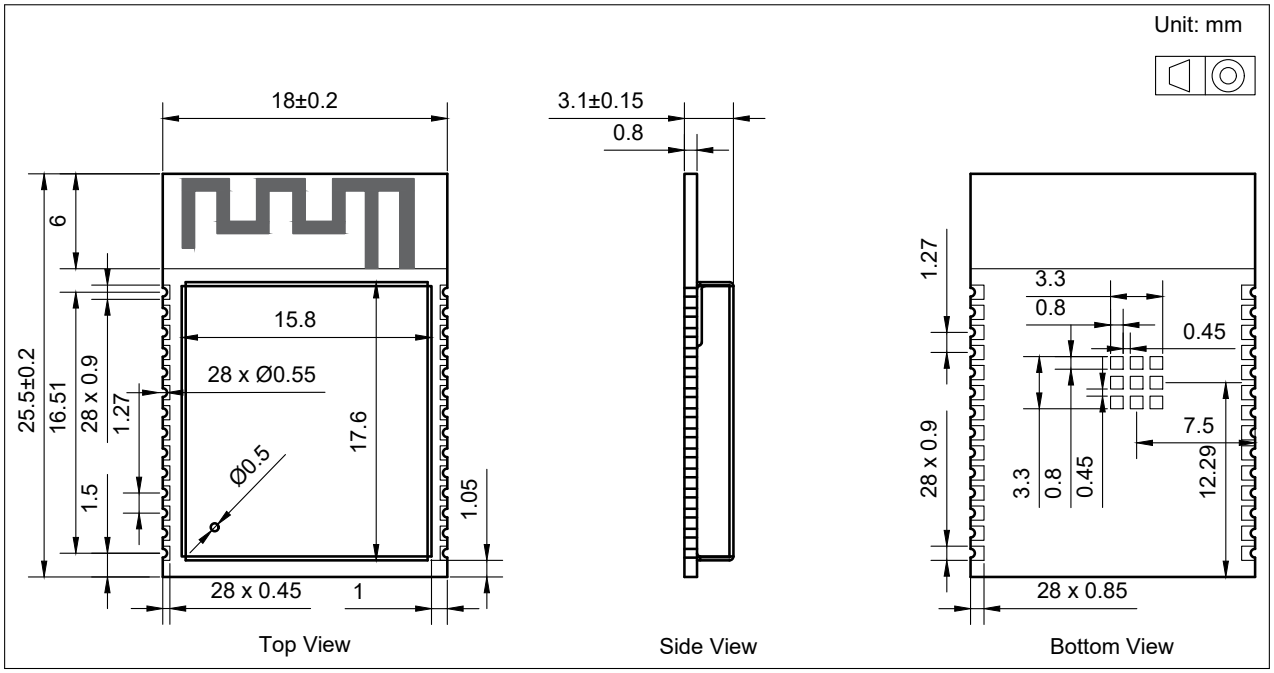

Figure 11: ESP32-C61-WROOM-1 Physical Dimensions

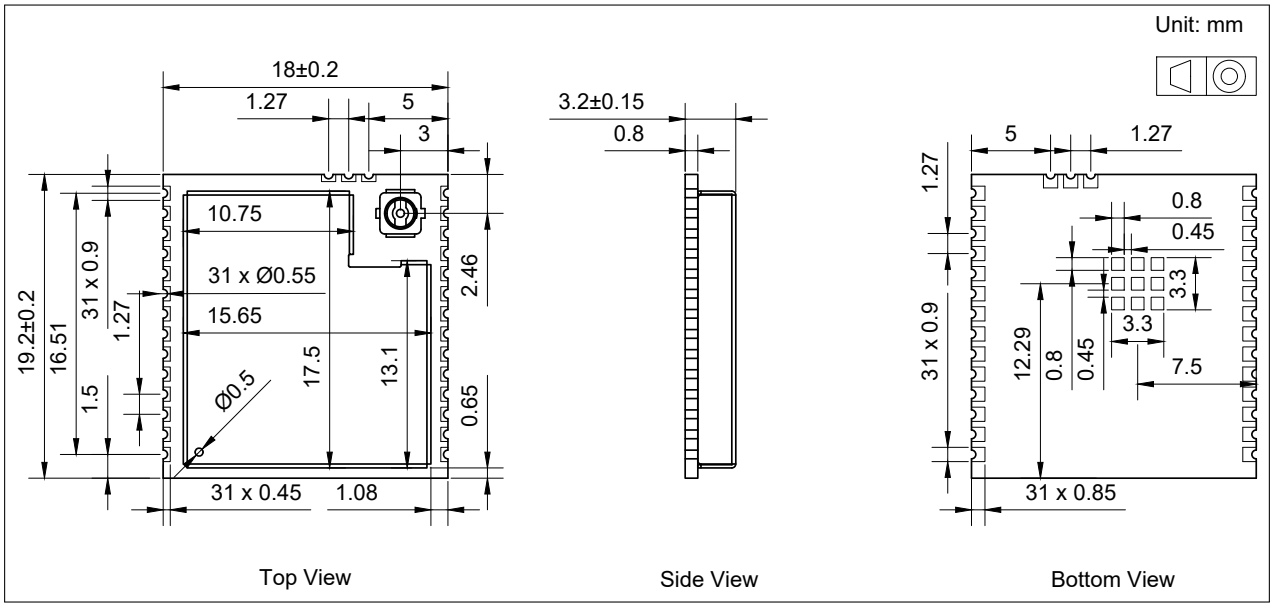

Figure 12: ESP32-C61-WROOM-1U Physical Dimensions

Note:
For information about tape, reel, and product marking, please refer to *ESP32-C61 Chip Packaging Information*.

10.2 Dimensions of External Antenna Connector

ESP32-C61-WROOM-1U uses the first generation external antenna connector as shown in Figure 13 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

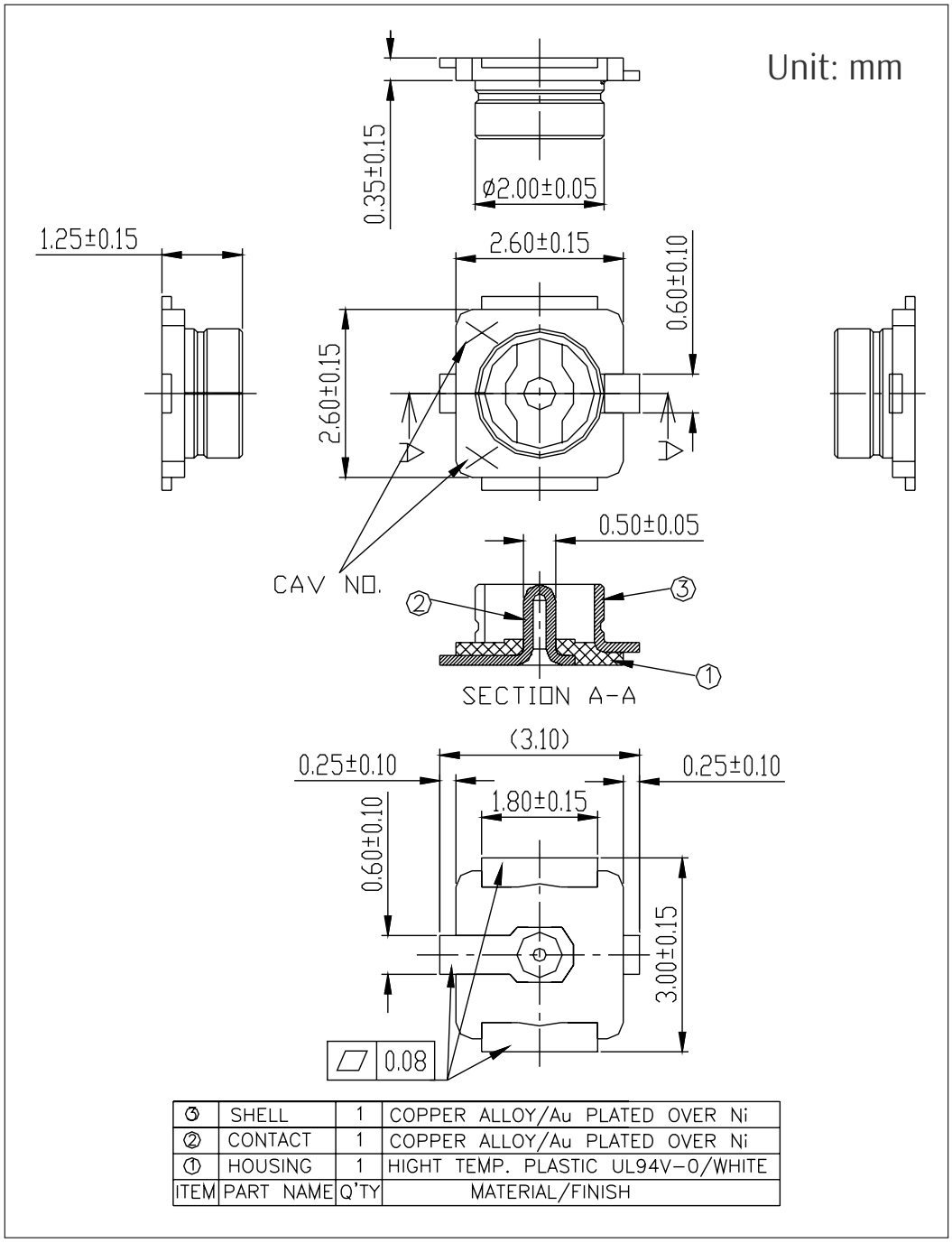

Figure 13: Dimensions of External Antenna Connector

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 14 *ESP32-C61-WROOM-1 Recommended PCB Land Pattern* and Figure 15 *ESP32-C61-WROOM-1U Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 14 and Figure 15 . You can view the source files for ESP32-C61-WROOM-1 and ESP32-C61-WROOM-1U with Autodesk Viewer.
- 3D models of ESP32-C61-WROOM-1 and ESP32-C61-WROOM-1U . Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

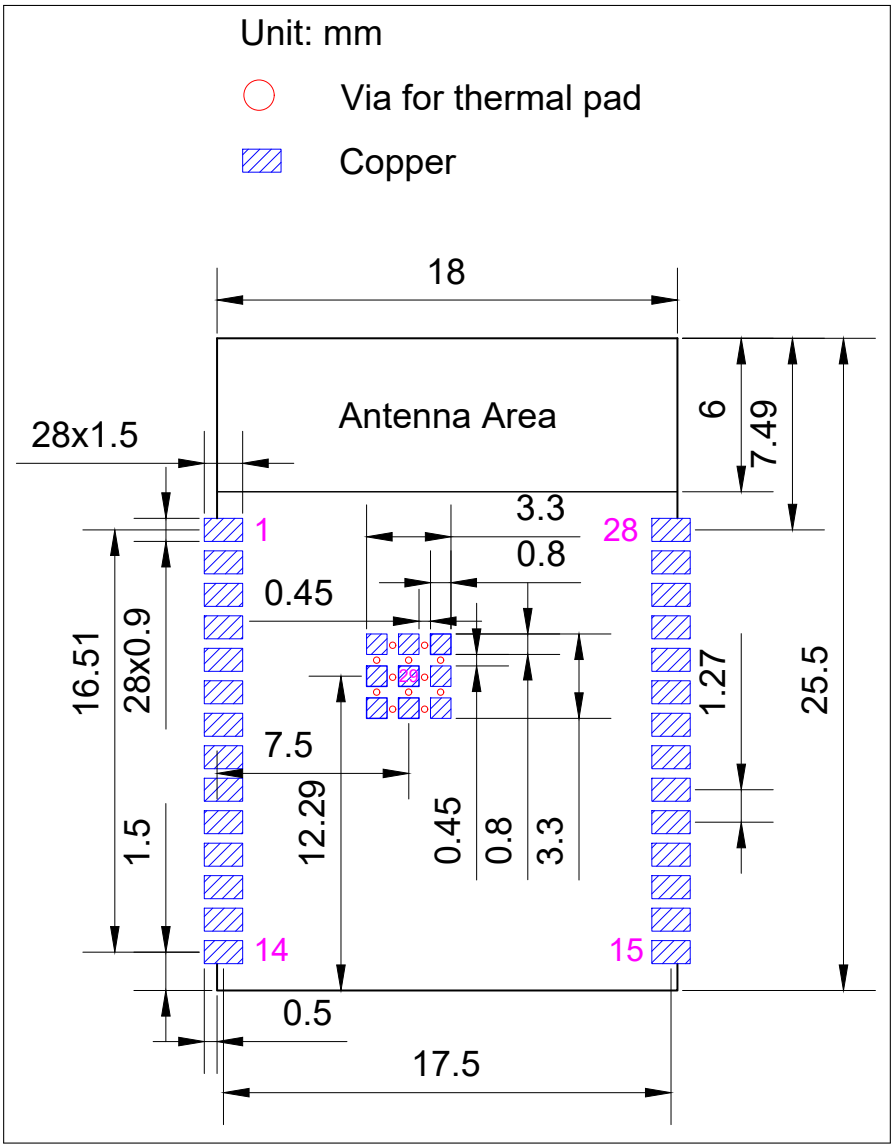

Figure 14: ESP32-C61-WROOM-1 Recommended PCB Land Pattern

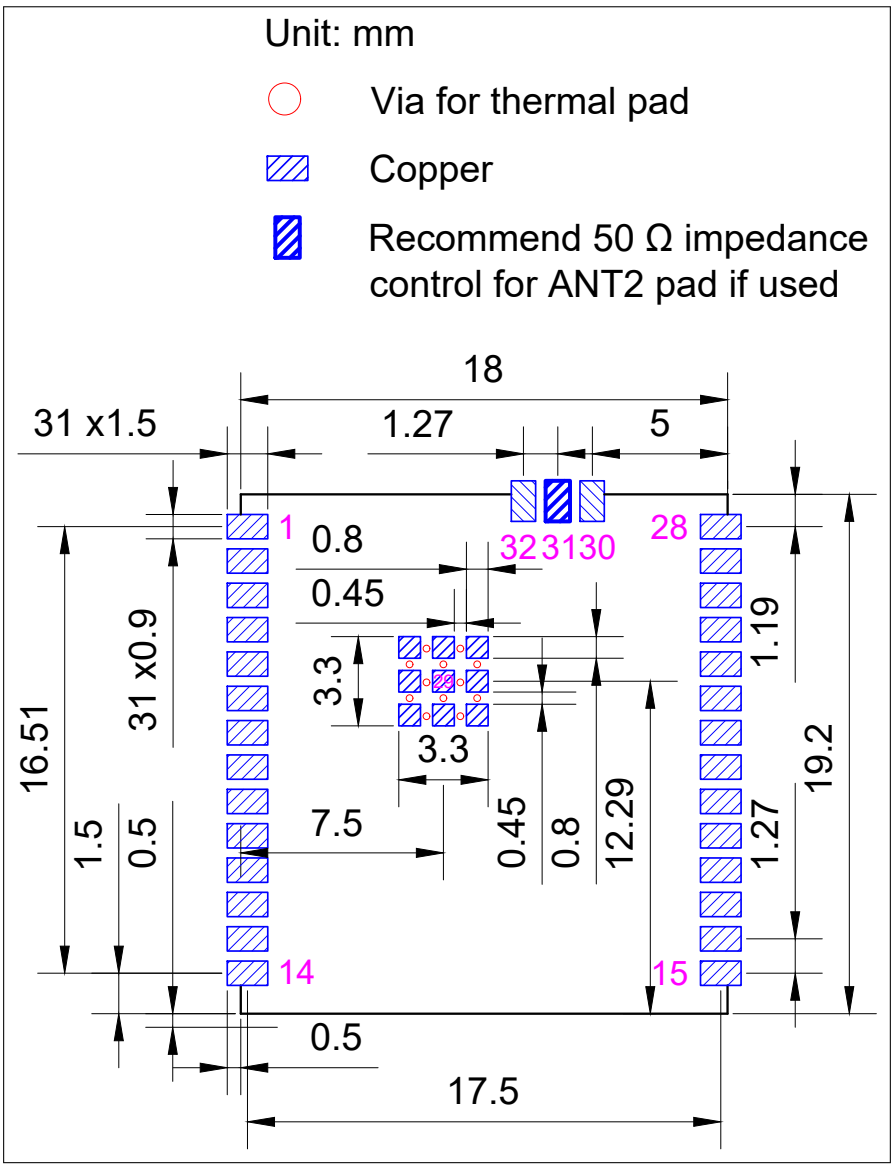

Figure 15: ESP32-C61-WROOM-1U Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-C61 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

12 Product Handling

12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

12.3 Reflow Profile

Solder the module in a single reflow.

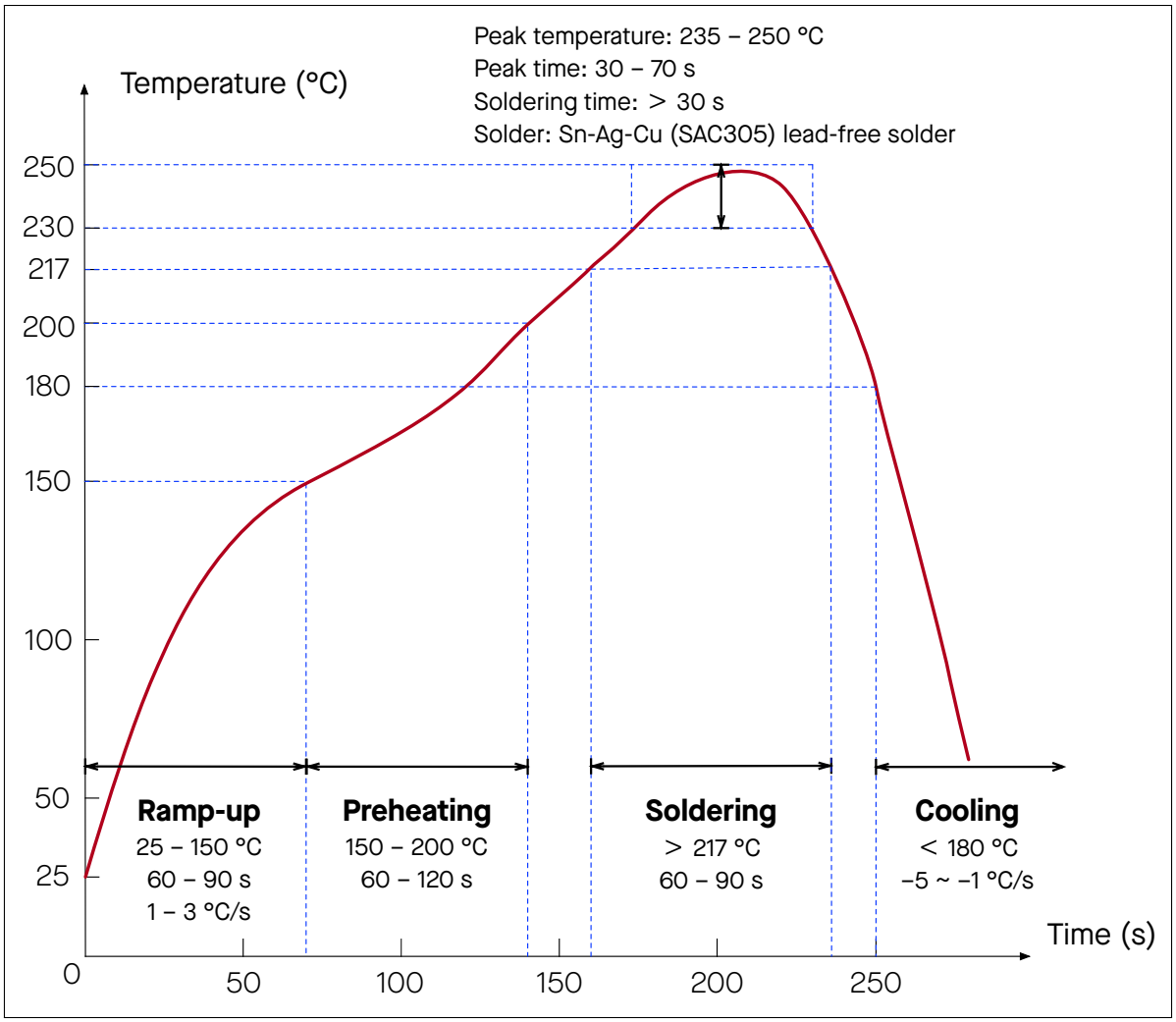

Figure 16: Reflow Profile

12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Related Documentation and Resources

Related Documentation

- ESP32-C61 Series Datasheet – Specifications of the ESP32-C61 hardware.
- ESP32-C61 Technical Reference Manual – Detailed information on how to use the ESP32-C61 memory and peripherals.
- ESP32-C61 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-C61 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-C61 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-C61
- *ESP32-C61 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-C61
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-C61 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-C61 Series SoCs* – Browse through all ESP32-C61 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C61
- *ESP32-C61 Series Modules* – Browse through all ESP32-C61-based modules.
  https://espressif.com/en/products/modules?id=ESP32-C61
- *ESP32-C61 Series DevKits* – Browse through all ESP32-C61-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-C61
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

Contact Us

- See the tabs *Sales Questions*, *Technical Enquiries*, *Circuit Schematic & PCB Design Review*, *Get Samples* (Online stores), *Become Our Supplier*, *Comments & Suggestions*.
  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2026-03-26	v1.1	Updated ESP32-C61-WROOM-1U Schematics of Chapter 8 Module Schematics
2025-12-30	v1.0	Official release
2025-09-09	v0.6	• Updated Chapter 8 Module Schematics • Updated Figure 6 *Visualization of Timing Parameters for the Strapping Pins*
2025-05-30	v0.5	First release

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